TIMING EQUIVALENCE CHECKING (TEC)
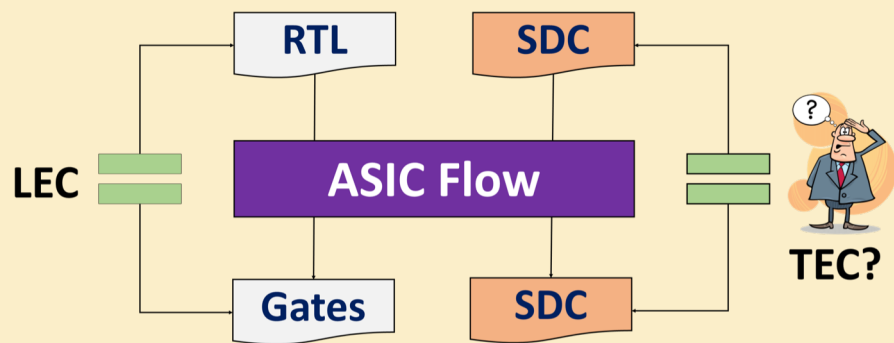
TIMING & LOGICAL EQUIVALENCY
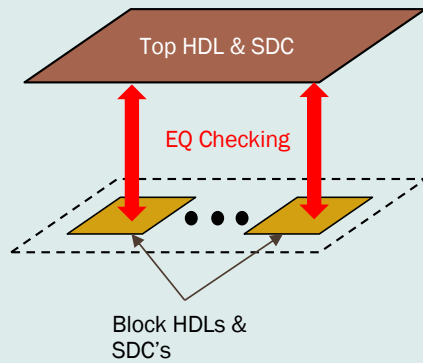

Chip design comprises of:
- Functionality
- Timing

No one tapes out without LEC

Why not TEC?

Timing Equivalence Checking
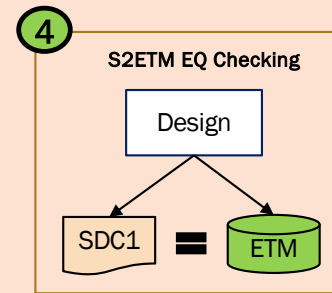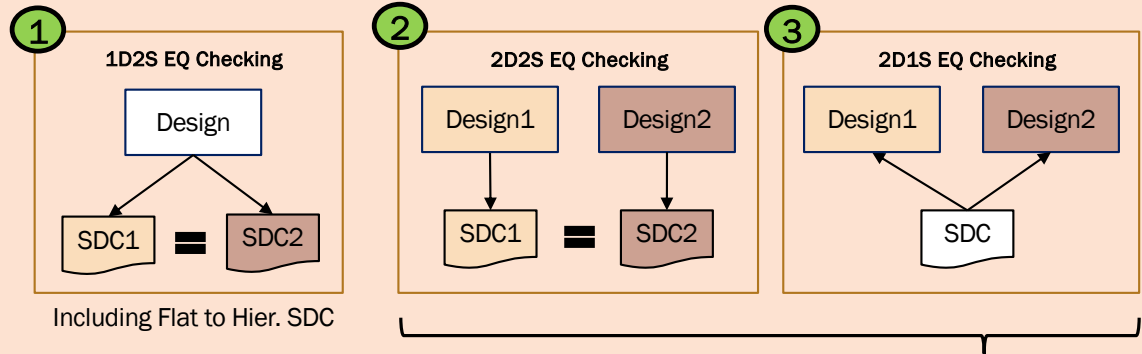
Extremely Dangerous to Tapeout Chip without running TEC
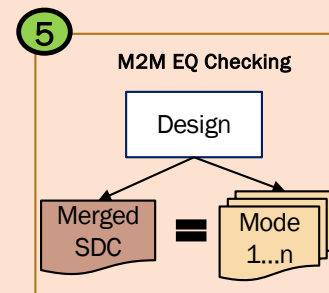
EQUIVALENCY & INSYNC CHECKING

Top2Block

Top HDL & SDC

EQ Checking

Block HDLs &
SDC's

Checks Equivalency of
Top level SDC against
Block level SDC's

Top2Top

1 1D2S EQ Checking

Design

SDC1 = SDC2

Including Flat to Hier. SDC

2 2D2S EQ Checking

Design1   Design2

SDC1 = SDC2

3 2D1S EQ Checking

Design1   Design2

SDC

4 S2ETM EQ Checking

Design

SDC1 = ETM

SDC to ETM equivalency
checking

5 M2M EQ Checking

Design

Merged SDC = Mode 1...n

Merged SDC to Multiple
Mode SDC equivalency
checking

2D2S & 2D1S

Includes support for the InSync Feature

Example of InSync: Effect of timing
constraints after design undergoes:
- ✓ Cloning
- ✓ Decloning/Merging
- ✓ Optimization out cells
- ✓ Buffering
- ✓ Pin Swapping
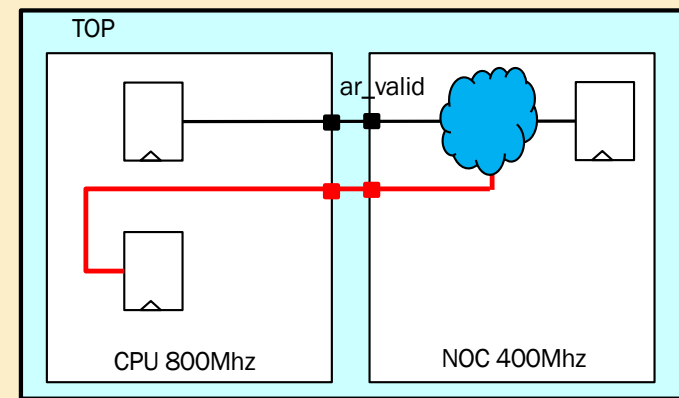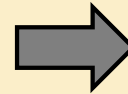- ✓ Logical Structuring
- ✓ ECO Changes

LOGICAL RESTRUCTURING WITH BOUNDARY OPTIMIZATION

- CPU clock is 800Mhz, NOC is 400MHz
- Paths between CPU & NOC are multicycle
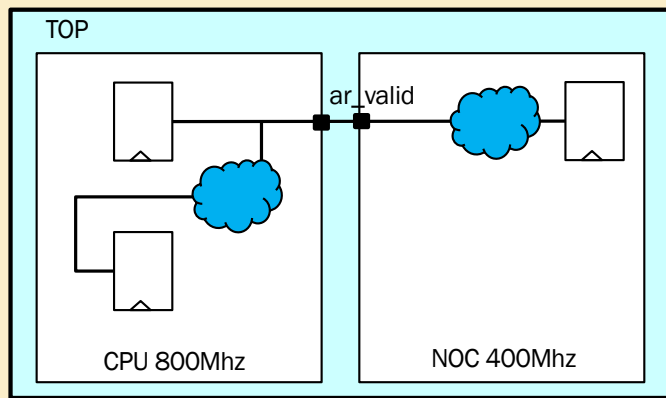
RTL

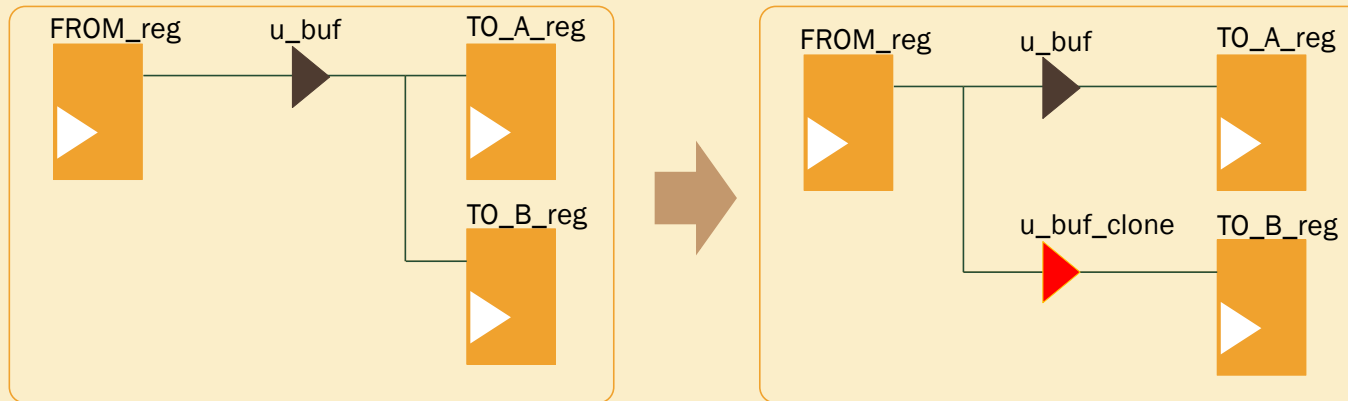*set_multicycle_path 2 –through noc/ar_valid*

After Synthesis

SDC generated after synthesis had the same *–through* multicycle

Synthesis created new ports and the path that was previously internal to the CPU is now going through the NOC *ar_valid* port and is also MCP'd

CLONING ON DATAPATH

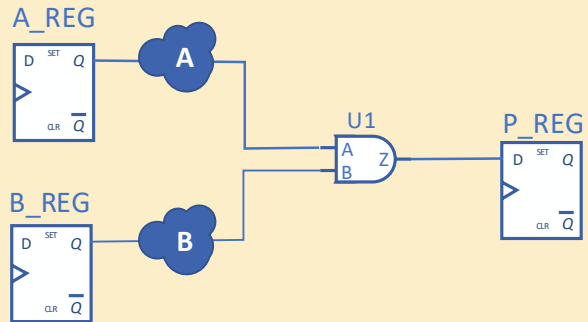*set_multicycle_path -start 2 -setup -through [get_cells u_buf]*

Before
FROM_reg -> TO_A_reg = setup:2 (multicycle path)
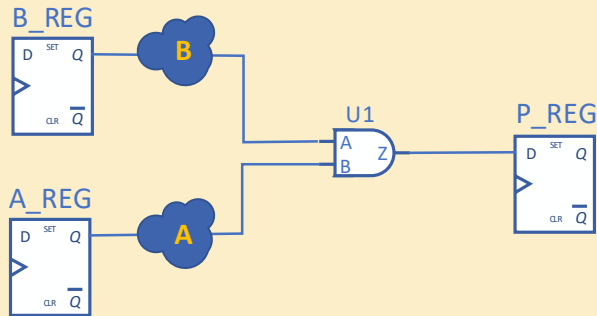FROM_reg -> TO_B_reg = setup:2 (multicycle path)

After
FROM_reg -> TO_A_reg = setup:2 (multicycle path)
FROM_reg -> TO_B_reg = setup:1

Use variable *cloning_map_pins* or *cloning_map_cells* to specify cloned pins/cells

PIN SWAPPING

set_false_path –through U1/A
All paths from A_REG to P_REG are False

set_false_path –through U1/A
*All paths from **B_REG** to P_REG are False*