Taiwan Semiconductor Manufacturing Company Limited

TSMC 20nm and CoWoS™ Design Infrastructure Ready

20nm and CoWoS™ Reference Flows enable next generation chip designs

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Hsinchu, Taiwan, R.O.C. – Oct. 9, 2012 – TSMC (TWSE: 2330, NYSE: TSM) announced today that the readiness of 20nm and CoWoS™ design support within the Open Innovation Platform® (OIP) is demonstrated by the delivery of two foundry-first reference flows supporting 20nm and CoWoS™ (Chip on Wafer on Substrate) technologies.

TSMC's 20nm Reference Flow enables double patterning technology (DPT) design using proven design flows. Leading EDA vendors' tools are qualified to work with TSMC 20nm process technology by incorporating DPT aware place and route, timing, physical verification and design for manufacturing (DFM). The new silicon-validated CoWoS™ Reference Flow that enables multi-die integration to support high bandwidth, low power can achieve fast time–to- market for 3D IC designs. The CoWoS™ flow also benefits designers by allowing them to use existing, mainstream tools from leading EDA vendors.

"These Reference Flows give designers access to TSMC's advanced 20nm and CoWoS technologies," said TSMC Vice President of R&D, Dr. Cliff Hou. "Delivering advanced silicon and manufacturing technologies as early and completely as possible to our customers is a chief goal for TSMC and its OIP design ecosystem partners."

20nm Reference Flow
TSMC's 20nm Reference Flow enables 20nm design with DPT aware capabilities to reduce design complexity and deliver required accuracy. DPT enablement includes pre-coloring capability, new RC extraction methodology, DPT sign-off, physical verification and DFM. In addition, TSMC and its ecosystem partners design 20nm IP for DPT compliance to accelerate 20nm process adoption.

CoWoS™ Reference Flow
The CoWoS™ Reference Flow enables 3D IC multi-die integration. The new CoWoS™ Reference Flow allows a smooth transition to 3D IC with minimal changes in existing methodologies. It includes the management of placement and routing of bumps, pads, interconnections, and C4 bumps; innovative combo-bump structure; accurate extraction and signal integrity analysis of high-speed interconnects between dies; thermal analysis from chip to package to system; and an integrated 3D testing methodology for die-level and stacking-level tests.

Custom Design Reference Flow and RF Reference Design Kit
The Custom Design Reference Flow enables DPT in 20nm custom layouts. It provides solutions to 20nm process requirements, including a direct link with simulators for the verification of voltage-dependent DRC rules, and integrated LDE solutions and handling of HKMG technology. RF Reference Design Kit provides new high frequency design guidelines. These consist of 60GHz RF model support, high

performance Electromagnetic (EM) characterization that enables customer design capability through the examples of 60GHz front-to-back implementation flow and Integrated Passive Device (IPD) support.

About Open Innovation Platform®

OIP promotes innovation for the semiconductor design community and ecosystem partners based on TSMC's complete technology portfolio. OIP includes a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that efficiently empower innovation throughout the supply chain, enabling the sharing of newly created revenue and profitability. OIP initiatives include reference flows, third-party IP validation, TSMC library IP, design kits and an online design portal.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry segment's largest portfolio of process-proven libraries, IPs, design tools and reference flows. The Company's managed capacity in 2011 totaled 13.22 million (8-inch equivalent) wafers, including capacity from three advanced 12-inch GIGAFAB™ facilities, four eight-inch fabs, one six-inch fab, as well as TSMC's wholly owned subsidiaries, WaferTech and TSMC China, and its joint venture fab, SSMC. TSMC is the first foundry to provide 28nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please visit http://www.tsmc.com.

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