Excellicon Timing Equivalence Checking (TEC) Capability Parallels Functional Equivalence; LEC, Addressing the GAP in the ASIC Flow.

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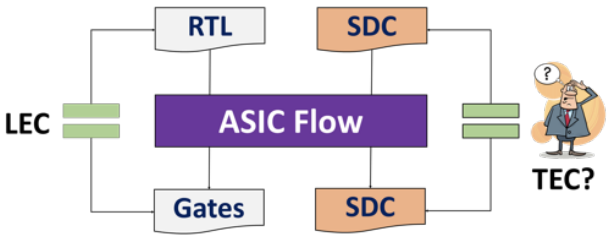
Excellicon Inc. an innovative provider of end-to-end timing constraints products announced full Equivalence checking capabilities for timing constraints. One of the biggest challenges in ensuring the consistency and completeness of timing constraints for any design, whether a derivative design or just reuse of earlier version of gate level timing constraints for the next generation of the same design, is to ensure the timing constraints are consistent across all layers of hierarchy and through all phases of the ASIC flow.

Timing Equivalence Checks (TEC) essentially closes a gap on the timing front, which has been covered on the functional side by functional equivalency tools; LEC.



Excellicon Timing Equivalence Checking (TEC) capability provide a comprehensive set of features to validate timing constraints for one design vs. two versions of timing constraints, or two designs and one timing constraints, or even two designs and two timing constraints.

Additionally, the product is capable of validating timing constraints between top level and lower level blocks for consistency and correctness, as well as checking for equivalency of a single merged mode vs. individual modes timing constraints, ETM model against the SDC.

"In recent years the timing constraints Equivalence checking has become as important as LEC for designers, since design reuse as well as design complexity has increased. Timing equivalence checking has become so important that design schedules are often significantly delayed in the absence of a solid methodology to consistently check the timing constraints for various versions of design throughout various stages of the ASIC flow." said Himanshu Bhatnagar, Excellicon's CEO.

About Excellicon

Excellicon is an innovative provider of end-to-end Timing Constraints Analysis and Debugging solutions for the automation of constraints authoring, completion, and validation from RTL to GDS with innovative analysis and debugging infrastructures. Excellicon products Constraints Manager, Constraints Certifier, Exception-ToolBox (ET), Budgeting-Tool Box (BT), Equivalence-Checker (EQ), and ConTree address the needs of designers at every stage of SOC design and implementation in a unified environment. – Timing Closure; Done Once! Done Right!

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