Timing and Power Optimization

ICExplorer-XTop

Timing closure is a major challenge for SoC designs, affecting both design quality and time to market. While dealing with huge timing data and making an optimization plan in a tight schedule, timing closure is a huge difficulty, especially in the advanced process.

ICExplorer-XTop provides a comprehensive timing closure solution. It can fix timing violations such as setup, hold, transition and leakage power in super large scale, multi-scenario, advanced node designs.

ICExplorer-XTop also has post-mask ECO, interactive ECO, and clock ECO to fix timing in the critical path and improve the efficiency of timing closure.

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Product

Complete Solution for Analog Design
Digital SoC Design Solution
Standard Cell Library Characterization
Standard Cell Library and IP Validation
Clock Diagnosis and Analysis
Timing and Power Optimization
Accurate Timing Simulation and Analysis
Layout Integration and Analysis
Complete Solution for Flat Panel Display Design
Foundry EDA Solution

Digital SoC Design Solution

Empyrean Technology provides a series of SoC solution including standard cell library characterization, standard cell library and IP validation, clock diagnosis and analysis, accurate timing simulation and analysis, timing and power optimization, and layout integration and analysis.

- Empyrean Liberal provides a solution for sign-off quality standard cell library characterization.
- Empyrean Qualib provides analysis and validation on standard cell library and IP to ensure design quality.
- Empyrean ClockExplorer provides clock diagnosis and analysis to reduces design reduce iterations and improves design cycles.
- ICExplorer-XTime provides a high accuracy timing analysis solution for advanced process and low voltage design. It brings a more efficient solution to the challenge of timing and design reliability in the advanced process and low voltage design.
- ICExplorer-XTop provides timing and power optimization for advanced process, large-scale and multi-scenario timing closures, including setup, hold, transition and leakage power optimization.
- Empyrean Skipper provides layout integration and analysis for ultra large scale layout, including fast loading and viewing of ultra large scale layout, fast layout integration, batch processing for layout, multi-threaded net tracing and point-to-point resistance analysis. It brings an efficient analysis and data processing solution to the ultra large-scale layout.

Testimonials

more 》

Renesas

SoC CTS

"Recent advanced designs have complicated clock structures to achieve higher performance and lower power cc makes it hard to detect the clock problems in a short period of time. Empyrean ClockExplorer can help to report C design stages such as pre-Place, pre-CTS, and post-CTS, with helpful...