Ncore™ Cache Coherent Interconnect IP

The Arteris IP Ncore Cache Coherent Interconnect IP offers unparalleled scalability, configurability and, with the optional Ncore Resilience package, data protection and hardware duplication capabilities to help achieve ISO 26262 ASIL D qualification for complex systems-on-chip (SoC).

Version 3 of the Ncore Cache Coherent Interconnect IP adds support for the AMBA CHI protocol as well as interoperability of CHI and ACE protocols in the same coherent system. In addition, CCIX interface support enables multi-die heterogeneous cache coherent systems. Ncore is scalable, supporting up to 16 coherent CPU clusters or other coherent agents. It incorporates multiple configurable snoop filters, multiple configurable proxy caches, and multiple configurable voltage and clock domains. All using a modular, distributed architecture for easier timing closure and place & route.

Benefits

ACCELERATE MACHINE LEARNING AND NEURAL NETWORK SOC DESIGNS

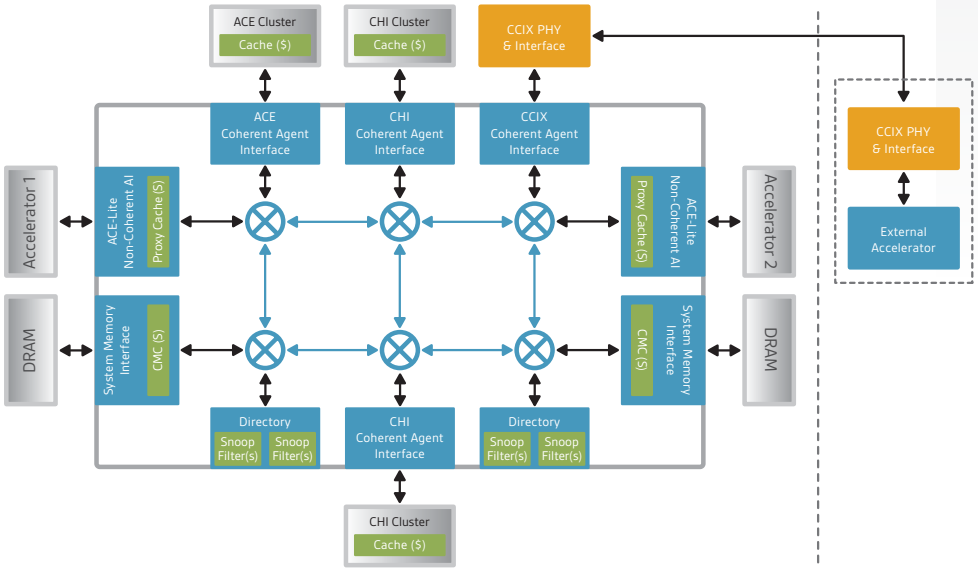
AMBA CHI and ACE interoperability allow more flexible integration of new and legacy processing elements, leveraging investments in existing ACE IP. Ncore's proxy caches allow more efficient use of die area than the dedicated SRAMs or scratchpad memories used in traditional pipelined neural network design, while also offering the means to simplify software.

DEVELOP ISO 26262-COMPLIANT COMPLEX SOCS

Achieving the desired ISO 26262 ASIL for a complex system is extremely difficult and often results in additional software burdens. Using the optional Ncore Resilience Package integrates hardware functional safety mechanisms in the interconnect, trapping errors and faults at the lowest possible level, and simplifying software and the FMEDA process.

SCALABILITY & FLEXIBILITY

Ncore Cache Coherent Interconnect IP scales up to 16 coherent agents, allowing for the design of highly flexible SoC platforms that can be tailored to meet changing product requirements. CCIX support enables multi-die heterogeneous cache coherent systems.



Fast Facts

- Supports up to 16 coherent agents or CPU clusters
- AMBA CHI and ACE interoperability
- CCIX support for multi-die cache coherent systems
- Low-latency proxy caches for efficient and quick integration of hardware accelerators into the coherent domain
- Configurable last level caches
- Meet ISO 26262 ASIL D requirements using the option Ncore resilience package with functional safety features including data protection, intelligent hardware duplication and fault controller

About Arteris IP

Arteris IP provides network-on-chip (NoC) interconnect IP to accelerate system-on-chip (SoC) semiconductor assembly for a wide range of applications from AI to automobiles, mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Samsung, Huawei / HiSilicon, Mobileye, and Texas Instruments. Arteris IP products include the Ncore cache coherent and FlexNoC non-coherent interconnect IP, the CodaCache standalone last level cache, and optional Resilience Package (ISO 26262 functional safety) and PIANO automated timing closure capabilities. Customer results obtained by using the Arteris IP product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at https://www.linkedin.com/company/arteris.

Leading Industry Perspectives

"We chose Ncore interconnect IP because of its outstanding configurability and flexibility, allowing us to create highly differentiated cache coherent SoCs using processors and accelerator IP optimized for the application. Having precise control over the configuration of coherent agent ports, memory interfaces, and snoop filters helps us make more power and area-efficient SoCs. The distributed hardware architecture allows for a more efficient physical design by easing backend placement and timing closure."

BENNY CHANG
VICE PRESIDENT OF R&D, AUTOMOTIVE MCU AND PROCESSORS BUSINESS LINE
NXP

"We chose the Arteris Ncore cache coherent interconnect because of its unique proxy caches and their ability to underpin high-performance, low power, cache coherent clusters of our unique AI accelerators. And with our prior experience using FlexNoC and the FlexNoC Resilience Packages for functional safety, we trust Arteris IP to be the highest performing and safest choice for ISO 26262-compliant NoC IP."

ELCHANAN RUSHINEK
VICE PRESIDENT OF ENGINEERING
MOBILEYE

"In evaluating cache coherent interconnects, we found that Arteris Ncore was the interconnect that provided us with the flexibility to fully optimize our system while also providing the data protection features we require to meet the highest possible ISO 26262 requirements. Arteris Ncore IP is a key component of our image recognition processor architecture."

NOBUAKI OTSUKA
SENIOR MANAGER, MIXED SIGNAL IC DESIGN DEPARTMENT
TOSHIBA

"Designers of machine-learning SoCs must integrate heterogeneous processor cores and accelerators into a complex system that can handle the high data bandwidth and low latency required for such applications. Arteris IP's new Ncore interconnect IP with resiliency features addresses these issues by enabling designers to implement heterogeneous cachecoherent machine-learning architectures for applications such as the rapidly developing autonomous-vehicle market."

MIKE DEMLER
SENIOR ANALYST
THE LINLEY GROUP

"The Arteris IP Ncore cache coherent interconnect not only allows the construction of a new class of automotive SoCs, but also implements safety mechanisms in hardware that increase the functional safety diagnostic coverage of the entire SoC. ArterisIP technology thus allows design teams to create highly complex SoCs that are capable of meeting the ISO 26262 ASIL D classification."

ANDREA BONDAVALLI
SCIENTIFIC ADVISOR
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