ES9218P

32-bit Stereo Mobile DAC with Headphone Amplifier, Analog Volume Control, and Output Switch

The ***ES9218P*** is a high-performance 32-bit, 2-channel audio **SABRE HiFi** D/A converter with QUAD DAC™ technology, headphone amplifier, analog volume control, and output switch designed for audiophile-grade portable applications such as mobile phones and digital music players, consumer applications such as USB DACs and A/V receivers, as well as professional applications such as mixer consoles and digital audio workstations.

Using critically acclaimed QUAD DAC™ technology, patented 32-bit HyperStream® DAC architecture and Time Domain Jitter Eliminator, the ***ES9218P*** delivers up to 121dB DNR and –114dB THD+N in HiFi mode, a performance level that will satisfy the most demanding audio enthusiasts.

The ***ES9218P's*** integrated SABRE DAC supports up to 32-bit 384kHz PCM and DSD256 audio data via master/slave I²S/DSD interface in synchronous and asynchronous sampling modes. A user-programmable FIR filter with 8 presets is included for customizable sound signature. Additionally, the ***ES9218P's*** integrated SABRE Headphone Amp supports up to 2.0Vrms output with analog gain control to reduce output noise at real-life listening levels. An integrated output switch allows an auxiliary source such as voice to bypass the ***ES9218P*** for lowest power consumption in non-HiFi mode. Residual distortion from suboptimal PCB components and layout can be minimized using ***ES9218P's*** unique THD compensation circuit, while PCB footprint and bill-of-material are minimized via the ***ES9218P's*** integrated feedback resistors and low-noise DAC reference LDO.

The ***ES9218P*** sets the standard for HD audio performance enabling **SABRE HiFi** experience all the way from the DAC to headphones for today's most demanding digital-audio applications in an easy-to-use 41-CSP package or 40 pin QFN package.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream II® DAC/HPA QUAD DAC™ technology +130dB SNR, +121dB DNR -114 dB THD+N, 1.0Vrms into 100kΩ -112 dB THD+N, 2.0Vrms into 300Ω -106 dB THD+N, 300mVrms into 32Ω	Industry's highest performance 32-bit mobile audio DAC/HPA with unprecedented dynamic range & ultra-low distortion Support synchronous and asynchronous sampling modes Enable SABRE HiFi experience all the way to headphones
Patented Time Domain Jitter Eliminator	Unmatched audio clarity free from input clock jitter
64-bit accumulator & 32-bit processing	Distortion free signal processing
Versatile digital input	Support master/slave PCM (I2S, LJ 16-32-bit), DSD or DoP
Customizable filter characteristics	8 preset filters User-programmable filter for custom sound signature
Output Switch for Auxiliary Source	Voice mode bypass with ultra-low power consumption
Integrated Low Noise AVCC LDO	Eliminate external LDO and reduce PCB size
Adjustable Analog Gain with Integrated HPA Feedback Resistors	Reduce noise at real-life listening levels Eliminate external thin film resistors and reduce PCB size
THD Compensation	Minimize DAC non-linearity
41-CSP Package and 40 pin QFN Package	Minimize PCB footprint
< 80mW quiescent power < 1mW standby power	Maximize battery life

APPLICATIONS

- Mobile phones / Tablets / Digital music players / Portable multimedia players
- Consumer and Audiophile USB DAC headphone amplifiers and A/V receivers
- Professional digital audio workstations and mixer consoles

Ordering Information

Part Number	Description	Package
ES9218PC	SABRE 32-bit Mobile Stereo DAC with Headphone Amplifier, Analog Volume Control, and Output Switch, on-chip feedback resistors	41-ball CSP
ES9218PQ	SABRE 32-bit Mobile Stereo DAC with Headphone Amplifier, Analog Volume Control, and Output Switch, on-chip feedback resistors	40 pin QFN

Revision History

Current Version 1.6

Rev.	Date	Notes
1.0	November 15, 2016	Initial release
1.1	December 9, 2016	Updated CSP Mechanical Dimensions
1.2	December 13, 2016	Register 8, GPIO Modes - Added OCP interrupts to list of interrupts. Changed name to "Interrupt" from "automute/lock interrupt" Register 11 - oc_sd_mute and oc_sd_gain descriptions Register 33 - Changed from reserved to Interrupt Mask. Added descriptions. Register 65 – Changed from reserved to ocbr and ocbl. Added descriptions. Register 72 - Changed oc_sd_mute description.
1.3	December 14, 2016	Added overcurrent protection to amplifier functional description. Removed notes with duplicate information from Serial Control Interface. Register 7 – Rename Corrected Minimum Phase Fast Roll-Off to Hybrid Fast Roll-Off Register 14 – Changed soft_start from reserved to supported. Register 33 – Separated 2bit registers into 1 bit registers. Register 46 – Corrected register bits and descriptions Register 48 – Changed hpa_hiq from reserved to supported. Register 55-56 – added missing register information. Register 65 – Separated 2 bit registers into 1 bit registers. Added description for clk_gear_rb Register 72 – Separated 2 bit registers into 1 bit registers. Corrected dop_status to dop_select. 41 Ball CSP Top View Marking updated
1.4	March 21, 2017	Added External Powered Oscillator/MCLK diagram, Crystal diagram, and Non-Optimal Crystal Circuitry diagram and explanation to Recommended Power Up Sequence section
1.5	November, 28, 2017	Removed ESS logo from 40-Pin QFN pin diagram.
1.6	February, 2, 2018	Update QUAD DAC™ notation