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(54) **AREA AND POWER EFFICIENT CIRCUITS FOR HIGH-DENSITY STANDARD CELL LIBRARIES**

(71) Applicant: **Samsung Electronics Co., Ltd.**, Suwon-si (KR)

(72) Inventors: **Sajal MITTAL**, Bengaluru (IN); **Abhishek GHOSH**, Bengalura (IN); **Utkarsh GARG**, Bengaluru (IN)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon-si (KR)

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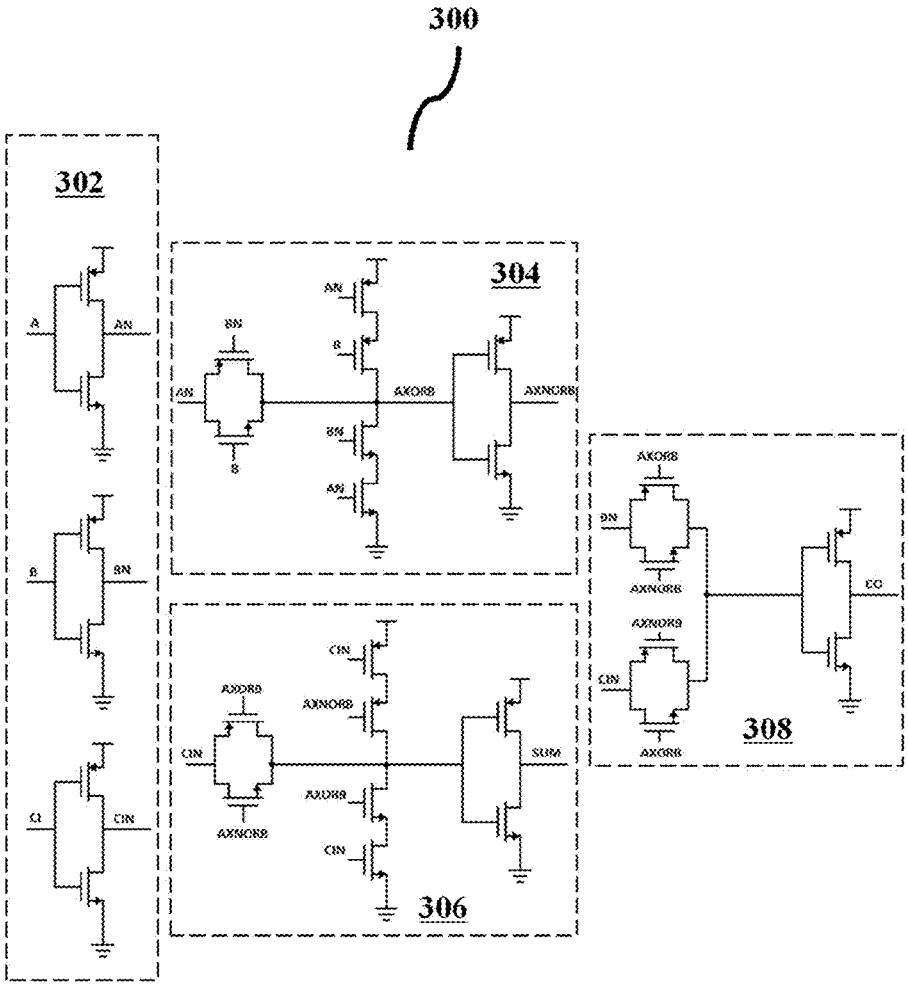
(57) **ABSTRACT**

Example embodiments provide a four input multiplexer integrated circuit (MXT4) associated with an integrated circuit (IC) and a method for reducing area and power of an integrated circuit (IC) using a MXT4, the MXT4 including a complementary signal generator circuit configured to receive first and second selection signals and to generate first and second complementary selection signals based on respective ones of the first and the second selection signals; and a p-type metal oxide semiconductor (PMOS) and an n-type metal oxide semiconductor (NMOS) stack switch circuit configured to transmit at least one input signal to an output based on the first and the second selection signals and the first and the second complementary selection signals.



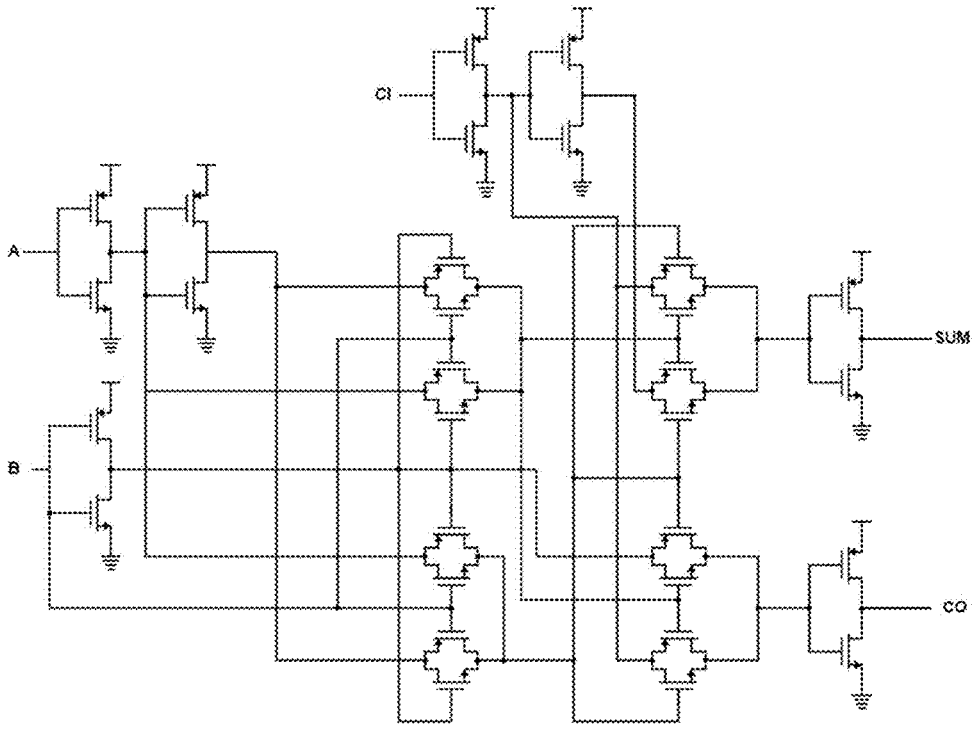


FIG.1
Related Art

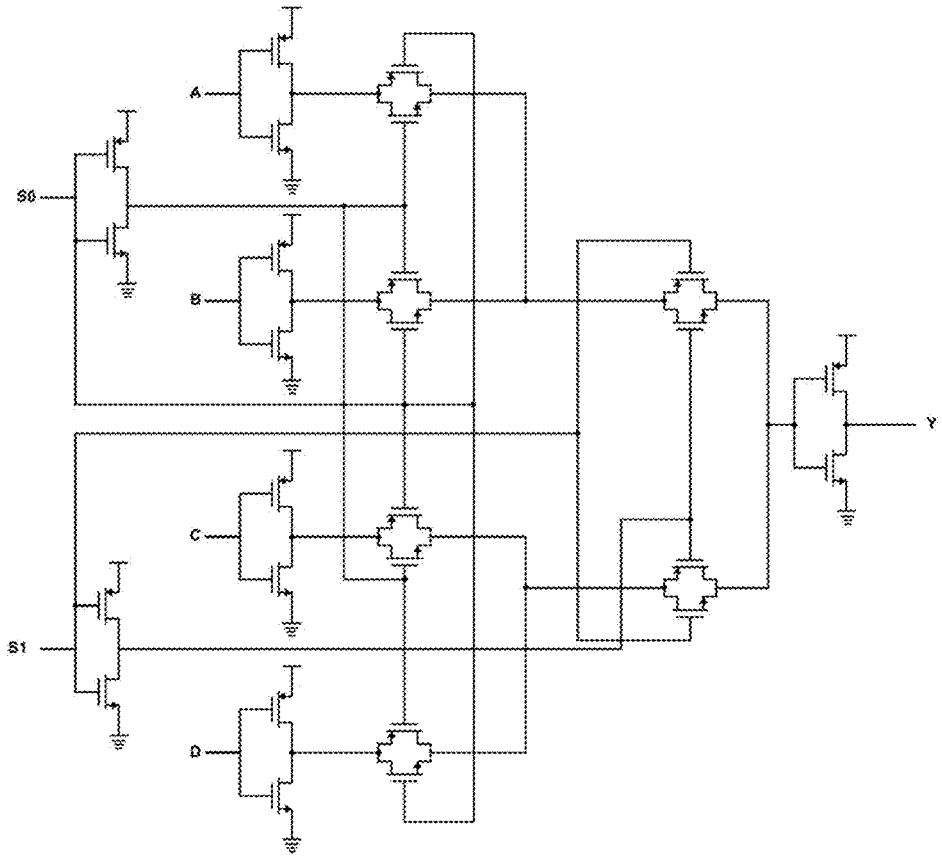


FIG.2
Related Art

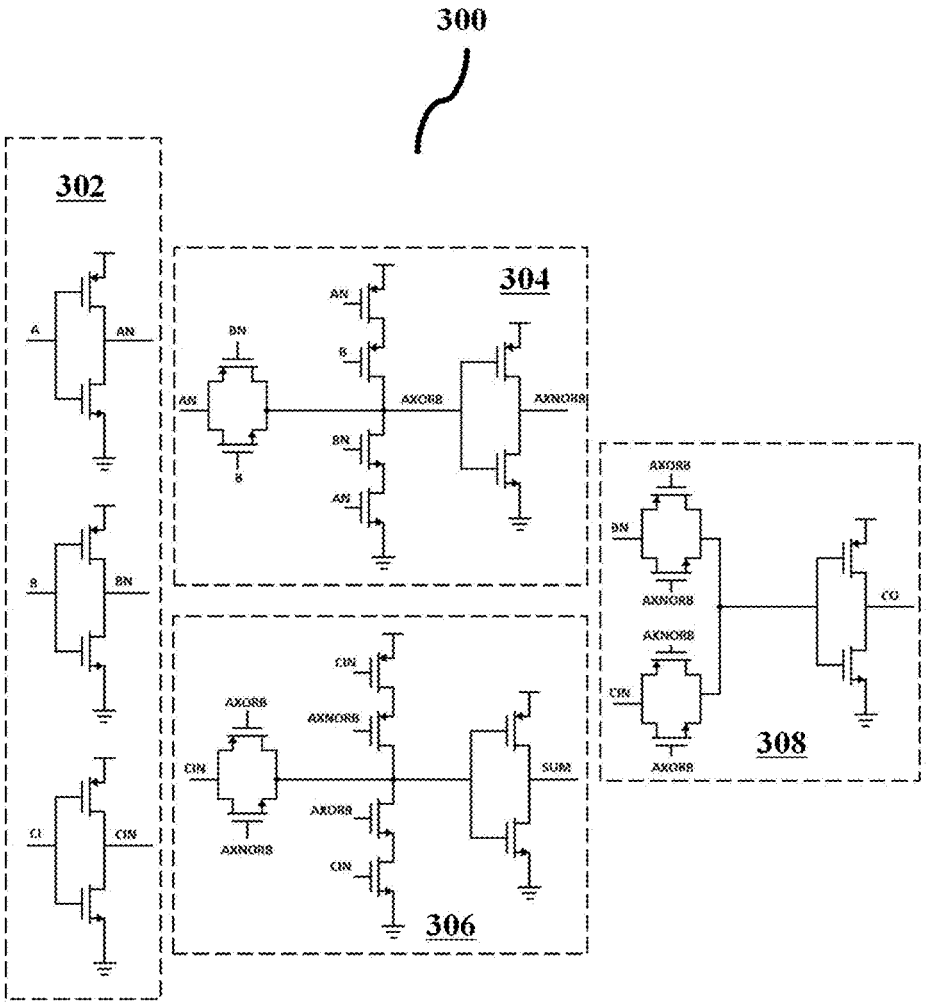


FIG.3

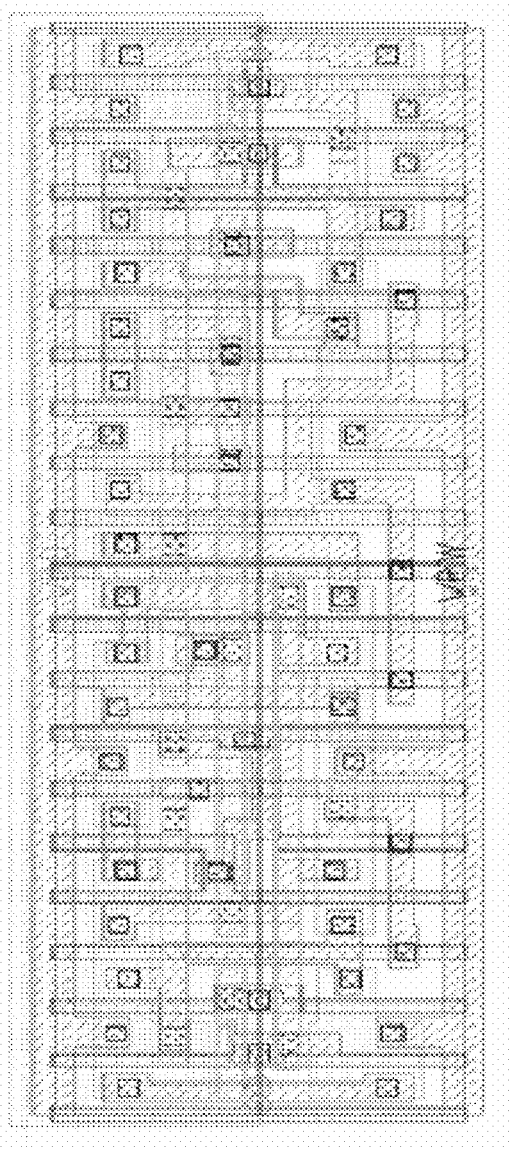


FIG. 4

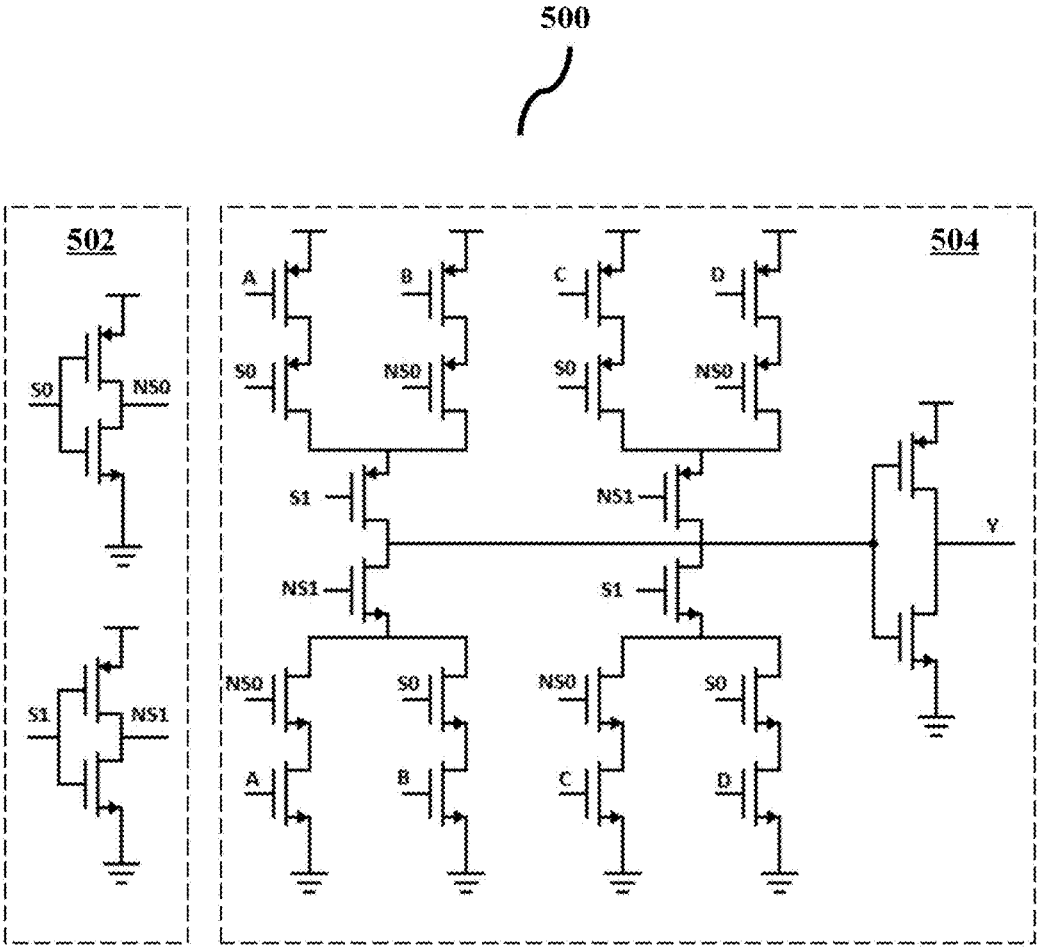


FIG.5

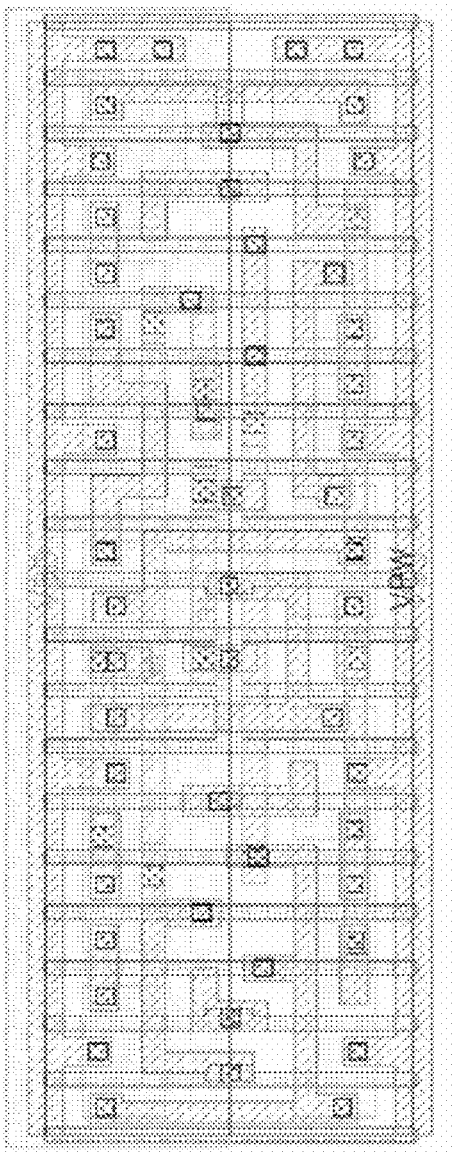


FIG. 6

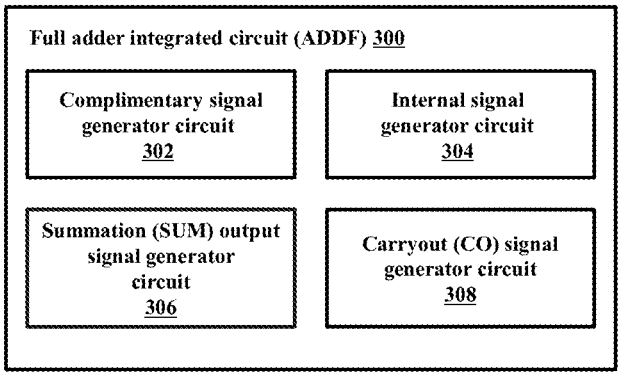

Full adder integrated circuit (ADDF) 300
Complimentary signal generator circuit 302
Internal signal generator circuit 304
Summation (SUM) output signal generator circuit 306
Carryout (CO) signal generator circuit 308

FIG.7

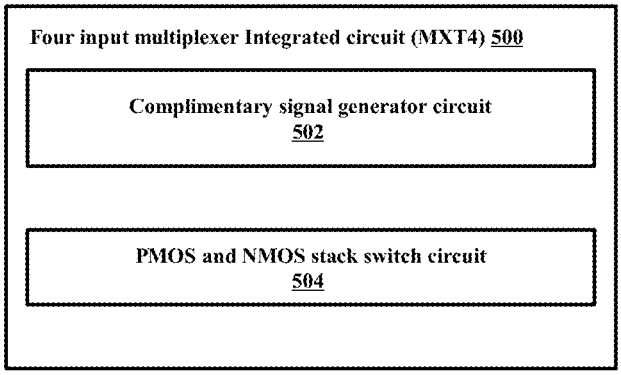

Four input multiplexer Integrated circuit (MXT4) 500
Complimentary signal generator circuit 502
PMOS and NMOS stack switch circuit 504

FIG.8

AREA AND POWER EFFICIENT CIRCUITS FOR HIGH-DENSITY STANDARD CELL LIBRARIES

[0001] This application is a divisional application of U.S. application Ser. No. 16/238,009, filed on Jan. 2, 2019, which claims the benefit of priority to India Patent Application 201841041881, filed on Nov. 5, 2018, in the India Intellectual Property Office, the disclosure of each of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] Example embodiments of the present disclosure relate to the field of semiconductor integrated circuits. For example, at least some example embodiments relate to producing an improved (or, alternatively, optimized) area and power efficient cell structures for high density standard cell libraries.

BACKGROUND

[0003] A common method of designing an integrated circuit (IC) may utilize a library of standard cells and a behavioral circuit model for describing the functionality of the IC. The standard cells typically include fundamental logic gates such as OR, NAND, NOR, AND, XOR, inverter, and like logical cells with an array of logic gate sizes. These cells also include sequential circuit elements such as latches and flip-flops for memory requirements. Generally, the library of standard cells are generated by a layout designer manually.

[0004] To design the ICs to utilize less area, high density standard cell libraries with area-efficient circuits may be used to help reduce area at block level. In design rule check (DRC) stringent technologies, each and every metal connection used in a layout causes routing congestion and results in higher area at the block level. Therefore, to improve (or, alternatively, optimize) the area at cell level, each and every circuit may need to be studied in an attempt to reduce (or, alternatively, minimize) the number of connections and improve (or, alternatively, maximize) the power sharing in layouts.

[0005] FIG. **1** illustrates a conventional full adder (ADDF) circuit, wherein the conventional ADDF circuit includes 8 transmission gates (TGs) and 7 inverters.

[0006] The conventional ADDF is based on the TGs, wherein an input A, B or CI is not directly given to the TGs, so that input capacitance for the circuit is constant and not changing with the input condition. Further, the conventional ADDF may utilize buffers for the inputs, which may increase area overhead. Further, the inputs are transmitted through the TGs depending upon the inputs. Due to large number of the TGs, there are extra metal connections in the layout which results in an area penalty. Depending upon the input signal conditions some of the transmission gates are ON and an input signal is transmitted and output summation (SUM) and carryout (CO) signals are generated.

[0007] FIG. **2** illustrates a conventional four input multiplexer (MXT4), where the input is inverted and transmitted through different TGs based on selection input signals. Due to a large number of TGs present in the conventional MXT4, there may be a large number of metal connections and a large routing complexity thus leading to area overhead. The conventional MXT4 has 6 input signals A, B, C, D, S**0** and S**1**. Hence depending upon the 4 input combinations of S**0** and S**1** signals, one of the input (A, B, C, D) signals goes to the output Y. Further, depending on the combination of S**0** and S**1**, transmission gates are ON and input is transmitted to the output Y.

SUMMARY

[0008] Example embodiments provide an area and power efficient full adder (ADDF) circuit and/or a 4-input multiplexer (MXT4) circuit for high density standard cell libraries.

[0009] At least some example embodiments herein provide a full adder (ADDF) circuit.

[0010] In some example embodiments, the ADDF includes a complementary signal generator circuit configured to receive three input signals and generate three complementary output signals based on respective ones of the three input signals, the three input signals each having one of a high logic level and a low logic level; an internal signal generator circuit configured to generate an internal signal based on two of the three complementary output signals and one of the three input signals; a summation output signal generator circuit configured to generate an output summation (SUM) signal based on one of the three complementary output signals, the internal signal and a complementary internal signal, the complementary internal signal being complementary to the internal signal; and a carryout signal generator circuit configured to generate a carry-out signal (CO) based on the two of the three complementary output signals, the internal signal and the complementary internal signal.

[0011] In an example embodiment, the ADDF uses less number of transmission gates (TGs) in the internal signal generator circuit and the SUM output signal generator circuit, thereby reducing surface area of the IC.

[0012] At least some other example embodiments herein provide a four input multiplexer integrated circuit (MXT4).

[0013] In some example embodiments, the MXT4 includes a complementary signal generator circuit configured to receive two selection input signals and to generate two complementary selection output signals based on respective ones of the two selection input signals; and a p-type metal oxide semiconductor (PMOS) and an n-type metal oxide semiconductor (NMOS) stack switch circuit configured to transmit at least one input signal to an output based on the two selection input signals and the two complementary selection output signals.

[0014] In an example embodiment, the MXT4 does not use any transmission gates (TGs), thereby reducing surface area of the IC.

[0015] At least some other example embodiments herein provide a method for reducing area and power of an integrated circuit (IC) using a full adder Integrated circuit (ADDF), the method comprising: generating, by a complementary signal generator circuit, three complementary output signals based on respective ones of three input signals, the three input signals each being one of a high logic level and a low logic level; generating, by an internal signal generator circuit, an internal signal based on two of the three complementary output signals, and one of the three input signals; generating, by a summation output signal generator circuit, an output summation (SUM) signal based on one of the three complementary output signals, the internal signal and a complementary internal signal, the complementary internal signal being complementary to the internal signal;

and generating, by a carryout signal generator circuit, a carry-out signal (CO) based on the two of the three complementary output signals, the internal signal and the complementary internal signal.

[0016] At least some other example embodiments herein provide a method generating, by a complementary signal generator circuit, two complementary selection output signals based on respective ones of two selection input signals; and transmitting, by a PMOS and a NMOS stack switch circuit, at least one input signal to an output based on the two selection input signals and the two complementary selection output signals.

[0017] These and other aspects of the example embodiments herein will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following descriptions, while indicating example embodiments and numerous specific details thereof, are given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the example embodiments herein without departing from the spirit thereof, and the example embodiments herein include all such modifications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Example embodiments herein are illustrated in the accompanying drawings, throughout which like reference letters indicate corresponding parts in the various figures. The example embodiments herein will be better understood from the following description with reference to the drawings, in which:

[0019] FIG. **1** illustrates a conventional full adder circuit;

[0020] FIG. **2** illustrates a conventional 4-input multiplexer (MXT4) circuit;

[0021] FIG. **3** illustrates a full adder (ADDF) circuit for high density standard cell libraries according to at least one example embodiment;

[0022] FIG. **4** illustrates a circuit layout of the ADDF circuit according to at least one example embodiment;

[0023] FIG. **5** illustrates 4-input multiplexer (MXT4) circuit for high density standard cell libraries according to at least one example embodiment;

[0024] FIG. **6** illustrates a circuit layout of the MXT4 circuit according to at least one example embodiment;

[0025] FIG. **7** is a block diagram illustrating various unit of the ADDF circuit according to at least one example embodiment; and

[0026] FIG. **8** is a block diagram illustrating various unit of the MXT4 circuit according to at least one example embodiment.

DETAILED DESCRIPTION

[0027] Example embodiments herein and the various features and advantageous details thereof are explained more fully with reference to the non-limiting example embodiments that are illustrated in the accompanying drawings and detailed in the following description. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the example embodiments herein. The description herein is intended merely to facilitate an understanding of ways in which the example embodiments herein can be practiced and to further enable those of skill in the art to practice the example embodiments herein. Accordingly, this disclosure should not be construed as limiting the scope of the example embodiments herein.

[0028] The example embodiments herein provide a full adder (ADDF) circuit for improving (or, alternatively optimizing) area and power of an integrated circuit (IC). The ADDF includes a complementary signal generator circuit to receive three input signals and generate corresponding complementary output signals for the received three input signals. The three input signals include at least one of a high logic level and a low logic level. Further, the ADDF includes an internal signal generator circuit to generate an internal signal using two complementary output signals out of the generated three corresponding complementary output signals, and one of the three input signals. Further, the ADDF includes a summation (SUM) output signal generator circuit to generate an output summation (SUM) signal using one complementary output signal out of the generated three corresponding complementary output signals, the generated internal signal and a complementary internal signal of the generated internal signal. Further, the ADDF include a carryout (CO) signal generator circuit configured to generate a carry-out signal (CO) using two complementary output signal out of the generated three corresponding complementary output signals, the generated internal signal and the complementary internal signal of the generated internal signal.

[0029] The example embodiments herein provide a four input multiplexer Integrated circuit (MXT4) for improving (or, alternatively, optimizing) area and power of an integrated circuit (IC). The MXT4 includes a complementary signal generator circuit to receive two selection input signals and generate corresponding complementary selection output signals for the received two selection input signals. Further, the MXT4 includes a p-type metal oxide semiconductor (PMOS) and a n-type metal oxide semiconductor (NMOS) stack switch circuit to transmit at least one input signal to an output based on the received two selection input signals and the generated corresponding two complementary selection output signals.

[0030] Referring now to the drawings, and more particularly to FIGS. **3** through **6**, where similar reference characters denote corresponding features consistently throughout the figures, there are shown some example embodiments.

[0031] FIG. **3** illustrates a full adder (ADDF) **300** circuit for high density standard cell libraries, according to at least one example embodiments, and FIG. **4** illustrates a circuit layout of the ADDF **300** circuit for high density standard cell libraries.

[0032] Referring to FIGS. **3** and **4**, in an example embodiment, the ADDF **300** may include a complementary signal generator circuit **302**, an internal signal generator circuit **304**, a summation (SUM) output signal generator circuit **306** and a carryout (CO) signal generator circuit **308**.

[0033] The complementary signal generator circuit **302** includes one or more inverters. The one or more inverters can be configured to receive three input signals A, B and CI, wherein the three input signals A, B and CI are adapted to take values either high logic level or low logic level. Further, the one or more inverters can be configured to generate three corresponding complementary output signals AN, BN and CIN based on the three input signals A, B and CI.

[0034] The internal signal generator circuit **304** includes combination of transmission gates, PMOS and NMOS stack and an inverter. The internal signal generator circuit **304** can

be configured to generate an internal signal AXORB using two complementary output signals (e.g., AN and BN) out of the three corresponding complementary output signals AN, BN and CIN and one of the three input signals (e.g., B). Further, the internal signal generator circuit **304** can be configured to generate a complementary internal signal (e.g., AXNORB).

[0035] The SUM output signal generator circuit **306** includes combination of transmission gates, a PMOS and a NMOS stack and an inverter. Further, the SUM output signal generator circuit **306** can be configured to generate an output SUM signal using one complementary output signal (e.g., CIN) out of the generated three corresponding complementary output signals AN, BN and CIN, the generated internal signal and the generated complementary internal signal of the generated internal signal.

[0036] The CO signal generator circuit **308** includes two inverter drivers for driving output signals. The CO signal generator circuit **308** can be configured to generate a carry-out signal (CO) using two complementary output signals (e.g., BN and CIN) out of the generated three corresponding complementary output signals AN, BN and CIN, the internal signal (e.g., AXORB) and the complementary internal signal (e.g., AXNORB) of the generated internal signal.

[0037] For example, the ADDF **300** can be configured to take 3-Input signals A, B and CI which can take values either high (Logic 1) or low (Logic 0). Hence, the ADDF **300** can be configured to receive a total of 8 input signal combinations. Further, the ADDF **300** can be configured to generate three complementary output signals depending on the input signals A, B and CI. The three complementary output signals includes AN, BN and CIN signals, which are complementary version of the input signals A, B and CI respectively. Further, the ADDF **300** can be configured to generate an internal signal for example, AXORB signal, which is generated based on the complementary output signals AN, BN and the input signal B. Further, the AXORB signal can be transmitted through an inverter and generates AXNORB signal, which is a complementary internal signal generated based on the internal signal. Further, a signal Z can be generated based on the signals CIN, AXORB and AXNORB. Further, the generated signal Z can be transmitted through the inverter and generates an output summation (SUM) signal. The output SUM signal has proper driver which provide glitch-less signal and which can be easily scalable. Similarly signal X is generated depending on the signals BN, CIN, AXORB and AXNORB. Further, the signal X can be transmitted through the inverter and generate output carry-out signal (CO).

[0038] FIG. **5** illustrates 4-input multiplexer (MXT4) circuit **500** for high density standard cell libraries, according to at least one example embodiment, and FIG. **6** illustrates a circuit layout of the MXT4 circuit for high density standard cell libraries.

[0039] Referring to FIGS. **5** and **6**, in an example embodiment, the MXT4 circuit **500** includes a complementary signal generator circuit **502** and a PMOS and a NMOS stack switch circuit **504**.

[0040] The complementary signal generator circuit **502** of the MXT4 circuit **500** can be configured to receive two selection input signals S**0** and S**1**, and to generate corresponding complementary selection output signals NS**0** and NS**1** based on respective ones of the two selection input signals S**0** and S**1**.

[0041] Further, depending on the selection input signal S**0** and S**1**, the PMOS and the NMOS stack switch circuit **504** can be configured to transmit at least one of input signal A, B C and D as an output signal Y. The selection signals S**0**, S**1**, NS**0** and NS**1** are used as a control signals for the NMOS's and the PMOS's stack.

[0042] In an example embodiment, based on the combination of S**0** and S**1**, the NMOS's and the PMOS's stack conducts and then the output signal Y can be pulled-down (goes to logic 0) or pulled-up (goes to logic 1) depending upon the at least one of input signals A,B, C and D.

[0043] The MXT4 circuit **500** doesn't use any of the input inverters, which is required only because of transmission gates (TGs). Since, the TGs are not used in the MXT4 design, which helps in closing the layout in lesser area.

[0044] FIG. **7** is a block diagram illustrating various unit of the ADDF **300** circuit, according to at least one example embodiment.

[0045] Referring to FIG. **7**, The ADDF **300** includes the complementary signal generator circuit **302**, the internal signal generator circuit **304**, the SUM output signal generator circuit **306** and the CO signal generator circuit **308**.

[0046] The complementary signal generator circuit **302** can be configured to receive three input signals A, B and C and generate three corresponding complementary output signals AN, BN and CIN based on respective ones of the three input signals A, B and C. The three input signals A, B and C each have one of the high logic level and the low logic level.

[0047] Further, the internal signal generator circuit **304** can be configured to generate an internal signal AXORB, BXORB or CXORB using two complementary output signals out of the three corresponding complementary output signals AN, BN and CIN, and one of the three input signals A, B and C.

[0048] The SUM output signal generator circuit **306** can be configured to generate an output SUM signal using one complementary output signal out of the three corresponding complementary output signals AN, BN and CIN, the internal signal AXORB, BXORB or CXORB and the complementary internal signal AXNORB, BXNORB or CXNORB associated with the internal signal AXORB, BXORB or CXORB.

[0049] The CO signal generator circuit **308** can be configured to generate a carry-out signal (CO) using two complementary output signals out of the three corresponding complementary output signals AN, BN and CIN, the generated internal signal AXORB, BXORB or CXORB and the complementary internal signal AXNORB, BXNORB or CXNORB associated with the internal signal AXORB, BXORB or CXORB.

[0050] The ADDF **300** can use less number of transmission gates (TGs) in the internal signal generator circuit **304** and the SUM output signal generator circuit **306**, thereby reduces surface area of the IC.

[0051] FIG. **8** is a block diagram illustrating various unit of the MXT4 circuit **500**, according to at least one example embodiment.

[0052] Referring to FIG. **8**, the MXT4 circuit **500** includes the complementary signal generator circuit **502** and the PMOS and the NMOS stack switch circuit **504**.

[0053] The complementary signal generator circuit **502** can be configured to receive two selection input signals S**0** and S**1** and generate two corresponding complementary

selection output signals NS0 and S1 based on respective ones of the two selection input signals S0 and S1.

[0054] Further, the PMOS and the NMOS stack switch circuit **504** can be configured to transmit at least one of input signals A, B, C or D as an output signal Y based on the two selection input signals S0, S1 and the two corresponding complementary selection output signals NS0 and NS1.

[0055] The MXT4 **500** does not use any transmission gates (TGs), thereby reduces surface area of the IC.

[0056] The example embodiments disclosed herein can be implemented through at least one software program running on at least one hardware device and performing network management functions to control the elements. The elements shown in FIG. **3** and FIG. **5** can be at least one of a hardware device, or a combination of hardware device and software module.

[0057] A standard cell included in an IC may be selected from a standard cell library including information about a plurality of standard cells, based on a physical characteristic of the standard cell such as a function and a timing characteristic. By placing an instance of the selected standard cell, a layout of the IC may be generated.

[0058] The standard cell library may include a high density standard cell library that includes the full adder (ADDF) circuit **300** for high density standard cell libraries according to at least one example embodiment and/or the 4-input multiplexer (MXT4) circuit **500** for high density standard cell libraries according to at least one example embodiment.

[0059] The high density standard cell library may include information about characteristics of a plurality of standard cells having different characteristics. For example, the high density standard cell library may include information about a power characteristic, a timing characteristic, or a shape characteristic of the ADDF circuit **300** and/or the 4-input multiplexer (MXT4) circuit **500** according example embodiments.

[0060] According to an example embodiment, a computing system for designing an IC may generate layout data of an IC with reference to the standard cell library.

[0061] The computing system may include the processor, the memory, an input/output (I/O) device, a storage device and a bus.

[0062] The processor may be configured, through a layout design or execution of computer readable instructions stored in the memory, as a special purpose computer to perform at least one of various operations of designing the IC.

[0063] The processor may communicate with the memory, the I/O device, and the storage device through the bus. The processor may design a layout of the IC by performing a logic synthesis operation, a design for testability (DFT) logic insertion operation, a placement and routing (P&R) operation, a parasitic component extraction operation and/or a static timing analysis (STA) operation.

[0064] The logic synthesis operation may generate a netlist from data defining functions of the IC in a hardware description language (HDL). The placing and routing (P&R) operation may generate layout data for the IC by placing and routing standard cells that define the IC according to the netlist. The static timing analysis (STA) operation may be performed on the layout data, and if the analysis passes, a mask may be generated based on the layout data.

[0065] The IC may be manufactured using the mask by performing various semiconductor processes on a semiconductor substrate such as a wafer to form the semiconductor device in which the IC is implemented. For example, a process using a mask may refer to a patterning process through a lithography process. Through such a patterning process, a desired pattern may be formed on a semiconductor substrate or a material layer. Meanwhile, the semiconductor processes may include a deposition process, an etching process, an ion process, a cleaning process, and the like. In addition, the semiconductor process may include a packaging process for mounting the semiconductor device on a printed circuit board (PCB) and sealing it with a sealing material, and may include a test process for testing the semiconductor device or a package.

[0066] The memory may be a volatile memory such as static random access memory (SRAM) or dynamic random access memory (DRAM), or may be a non-volatile memory such as phase-change random access memory (PRAM), magnetoresistive random access memory (MRAM), resistive random access memory (ReRAM), ferroelectric random access memory (FRAM), or NOR flash memory.

[0067] The I/O device may control a user input and an output performed through user interface devices. For example, the I/O device may include one or more input devices such as a keyboard, a mouse device, and a touch pad and may receive input data which defines the IC. For example, the I/O device may include output devices such as a display and a speaker and may display a placement result, a routing result, an STA result, etc.

[0068] The storage device may include a memory card (for example, multimedia card (MMC), an embedded multimedia card (eMMC), a secure digital (SD) card, a MicroSD card, etc.), a solid state drive (SSD), a hard disk drive (HDD), and/or the like.

[0069] The foregoing description of some of the example embodiments will so fully reveal the general nature of the example embodiments herein that others can, by applying current knowledge, readily modify and/or adapt such specific example embodiments without departing from the example embodiments, and, therefore, such adaptations and modifications should and are intended to be comprehended within the meaning and range of equivalents of the disclosed example embodiments. It is to be understood that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Therefore, while the example embodiments herein have been described in terms of some example embodiments, those skilled in the art will recognize that the example embodiments herein can be practiced with modification within the spirit and scope of the example embodiments as described herein.

What is claimed is:

1. A four input multiplexer integrated circuit (MXT4) associated with an integrated circuit (IC), the MXT4 comprising:

a complementary signal generator circuit configured to receive first and second selection signals and to generate first and second complementary selection signals based on respective ones of the first and the second selection signals; and

a p-type metal oxide semiconductor (PMOS) and an n-type metal oxide semiconductor (NMOS) stack switch circuit configured to transmit at least one input signal to an output based on the first and the second selection signals and the first and the second complementary selection signals.

2. The MXT4 of claim 1, wherein the complementary signal generator circuit includes one or more inverters.

3. The MTX4 of claim 2, wherein the one or more inverters of the complementary signal generator circuit include two inverters configured to receive the respective ones of the first and the second selection signals without the first and the second input signals being passed through buffers, and to generate the first and the second complementary selection signals.

4. The MTX4 of claim 1, wherein the PMOS and NMOS stack switch circuit is configured to receive first to fourth input signals, and to transmit one of the first to the fourth input signals to the output based on the first and the second selection signals and the first and the second complementary selection signals.

5. The MTX4 of claim 4, wherein the PMOS and NMOS stack switch circuit is configured to transmit one of the first to the fourth input signals to the output without the first to the fourth input signal being passed through a transmission gate.

6. The MTX4 of claim 4, wherein the PMOS and NMOS stack switch circuit comprises:

first to fourth PMOS transistors connected to a source, the first to fourth PMOS transistors configured to receive the first to the fourth input signals, respectively; and

first to fourth NMOS transistors connected to a ground, the first to fourth NMOS transistors configured to receive the first to the fourth input signals, respectively, wherein

the first to the fourth input signals are only provided to a circuit including the first to the fourth PMOS transistors and the first to the fourth NMOS transistors.

7. The MTX of claim 6, wherein the PMOS and NMOS stack switch circuit further comprises:

fifth and sixth PMOS transistors connected to the first and the third PMOS transistors in series, respectively, the fifth and sixth PMOS transistors configured to receive the first selection signal;

seventh and eighth PMOS transistors connected to the second and the fourth PMOS transistors in series, respectively, the seventh and eighth PMOS transistors configured to receive the first complementary selection signal;

fifth and sixth NMOS transistors connected to the first and the third NMOS transistors in series, respectively, the fifth and sixth NMOS transistors configured to receive the first complementary selection signal; and

seventh and eighth NMOS transistors connected to the second and the fourth NMOS transistors in series, respectively, the seventh and eighth NMOS transistors configured to receive the first selection signal, wherein

the first selection signal and the first complementary selection signal are only provided to a circuit including the fifth to the eighth PMOS transistors and the fifth to the eighth NMOS transistors.

8. The MTX of claim 7, wherein the PMOS and NMOS stack switch circuit further comprises:

a ninth PMOS transistor connected to the fifth and the seventh PMOS transistors at a first node, the ninth PMOS transistor configured to receive the second selection signal;

a tenth PMOS transistor connected to the sixth and the eighth PMOS transistors at a second node, the tenth PMOS transistor configured to receive the second complementary selection signal;

a ninth NMOS transistor connected to the fifth and the seventh NMOS transistors at a third node, the ninth NMOS transistor configured to receive the second complementary selection signal; and

a tenth NMOS transistor connected to the sixth and the eighth NMOS transistors at a fourth node, the tenth NMOS transistor configured to receive the second selection signal, wherein

the second selection signal and the second complementary selection signal are only provided to a circuit including the ninth and the tenth PMOS transistors and the ninth and the tenth NMOS transistors.

9. The MTX of claim 8, wherein the ninth and the tenth PMOS transistors and the ninth and the tenth NMOS transistors are connected to a fifth node, and the PMOS and NMOS stack switch circuit further comprises:

an inverter having an input connected to the fifth node, the inverter configured to generate an output signal at the output.

10. A method for reducing area and power of an integrated circuit (IC) using a four input multiplexer Integrated circuit (MXT4), the method comprising:

generating, by a complementary signal generator circuit, first and second complementary selection signals based on respective ones of first and second selection signals; and

transmitting, by a PMOS and a NMOS stack switch circuit, at least one input signal to an output based on the first and the second selection signals and the first and the second complementary selection signals.

11. The method of claim 10, wherein the generating the first and the second complementary selection signals comprises:

generating the first and the second complementary selection signals based on the respective ones of first and second selection signals without the first and the second selection signals passing through buffers.

12. The method of claim 10, wherein the transmitting the at least one input signal to the output comprises:

receiving first to fourth input signals, the first and the second selection signals, and the first and the second complementary signals; and

transmitting one of the first to the fourth input signals to the output based on the first and the second selection signals, and the first and the second complementary signals.

13. The method of claim 12, wherein the transmitting one of the first to the fourth input signals to the output comprises:

transmitting one of the first to the fourth input signals to the output based on the first and the second selection signals, and the first and the second complementary signals without the first to the fourth input signal being passed through a transmission gate.

14. The method of claim 12, wherein the receiving the first to the fourth input signals, the first and the second selection signals, and the first and the second complementary signals comprises:

providing the first to the fourth input signals to first to fourth PMOS transistors, respectively; and

providing the first to the fourth input signals to first to fourth NMOS transistors, respectively, wherein

the first to the fourth input signals are only provided to a circuit including the first to the fourth PMOS transistors and the first to the fourth NMOS transistors.

15. The method of claim **14**, wherein the receiving the first to the fourth input signals, the first and the second selection signals, and the first and the second complementary signals comprises:

providing the first selection signal to fifth and sixth PMOS transistors connected to the first and the third PMOS transistors, respectively;

providing the first complementary selection signal to seventh and eighth PMOS transistors connected to the second and the fourth PMOS transistors, respectively;

providing the first complementary selection signal to fifth and sixth NMOS transistors connected to the first and the third NMOS transistors, respectively; and

providing the first selection signal to seventh and eighth NMOS transistors connected to the second and the fourth NMOS transistors, respectively, wherein

the first selection signal and the first complementary selection signal are only provided to a circuit including the fifth to the eighth PMOS transistors and the fifth to the eighth NMOS transistors.

16. The method of claim **15**, wherein the receiving the first to the fourth input signals, the first and the second selection signals, and the first and the second complementary signals comprises:

providing the second selection signal to ninth PMOS transistor connected to a source via the first and the fifth PMOS transistors and via the second and the seventh PMOS transistors;

providing the second complementary selection signal to tenth PMOS transistor connected to the source via the third and the sixth PMOS transistors and via the fourth and the eighth transistors;

providing the second complementary selection signal to ninth NMOS transistor connected to a ground via the first and the fifth NMOS transistors and via the second and the seventh NMOS transistors; and

providing the second selection signal to tenth NMOS transistor connected to the ground via the third and the sixth NMOS transistors and via the fourth and the eighth NMOS transistors, wherein

the second selection signal and the second complementary selection signal are only provided to a circuit including the ninth and tenth PMOS transistors and the ninth and the tenth NMOS transistors.

17. The method of claim **16**, wherein the ninth and the tenth PMOS transistors, and the ninth and the tenth NMOS transistors are commonly connected at an internal node, and wherein the transmitting one of the first to the fourth input signals to the output comprises:

generate an output signal at the output by inverting an internal signal of the internal node.

18. A four input multiplexer integrated circuit (MXT4) associated with an integrated circuit (IC), the MXT4 comprising:

a complementary signal generator circuit configured to receive first and second selection signals, and to generate first and second complementary selection signals by inverting the first and the second selection signals, respectively; and

first to fourth PMOS stacks configured to receive first to fourth input signals, respectively, and to receive one of the first selection signal and the first complementary selection signal;

first to fourth NMOS stacks configured to receive the first to fourth input signals, respectively, and to receive one of the first selection signal and the first complementary selection signal;

a first PMOS and NMOS stack and a second PMOS and NMOS stack, the first PMOS and NMOS stack and the second PMOS and NMOS stock each configured to receive the second selection signal and the second complementary selection signal; and

an inverter configured to receive an internal signal from the first stack and the second stack, and to generate an output signal at an output.

19. The MXT4 of claim **18**, wherein

the first PMOS stack and the second PMOS stack are connected in parallel between a source and a first node,

the third PMOS stack and the fourth PMOS stack are connected in parallel between the source and a second node,

the first NMOS stack and the second NMOS stack are connected in parallel between a ground and a third node, and

the third NMOS stack and the fourth NMOS stack are connected in parallel between the ground and a fourth node.

20. The MXT4 of claim **19**, wherein

the first PMOS and NMOS stack is connected between the first node and the third node, and

the second PMOS and NMOS stack is connected between the second node and the fourth node.

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