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(54) **HIGH-FREQUENCY AMPLIFIER
CIRCUITRY AND SEMICONDUCTOR
DEVICE**

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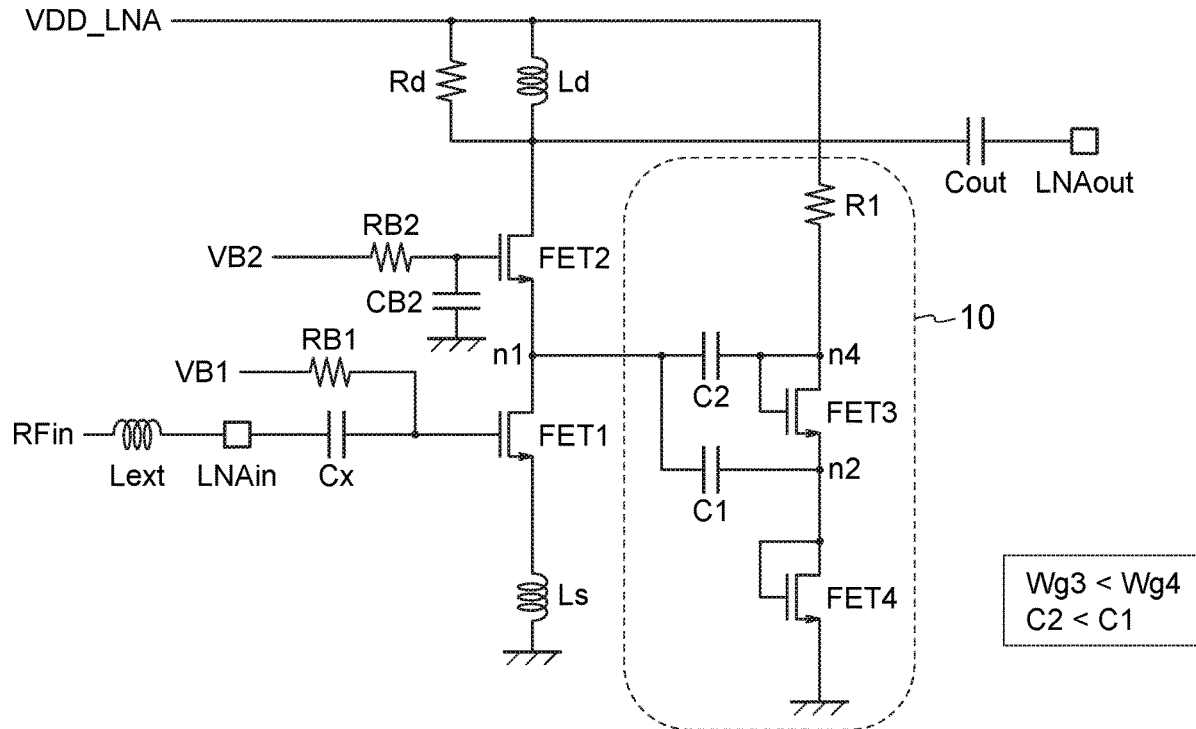
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(57) **ABSTRACT**

Circuitry includes an amplifier circuit having a first transistor, an inductor, and a second transistor, and a distortion compensation circuit having a third transistor, a fourth transistor, and a first capacitor. The first transistor is applied input signal. The inductor is connected to a source of the first transistor and grounded on another side. The second transistor has a source connected to a drain of the first transistor, a grounded gate and a drain connected to a power supply, and outputs an amplified signal. The third transistor has a drain and a gate connected to the drain, and is connected to the power supply on the drain. The fourth transistor has a drain and a gate connected to a source of the third transistor, and is grounded on a source. The first capacitor connects nodes between the drain of the first transistor and the source of the third transistor.



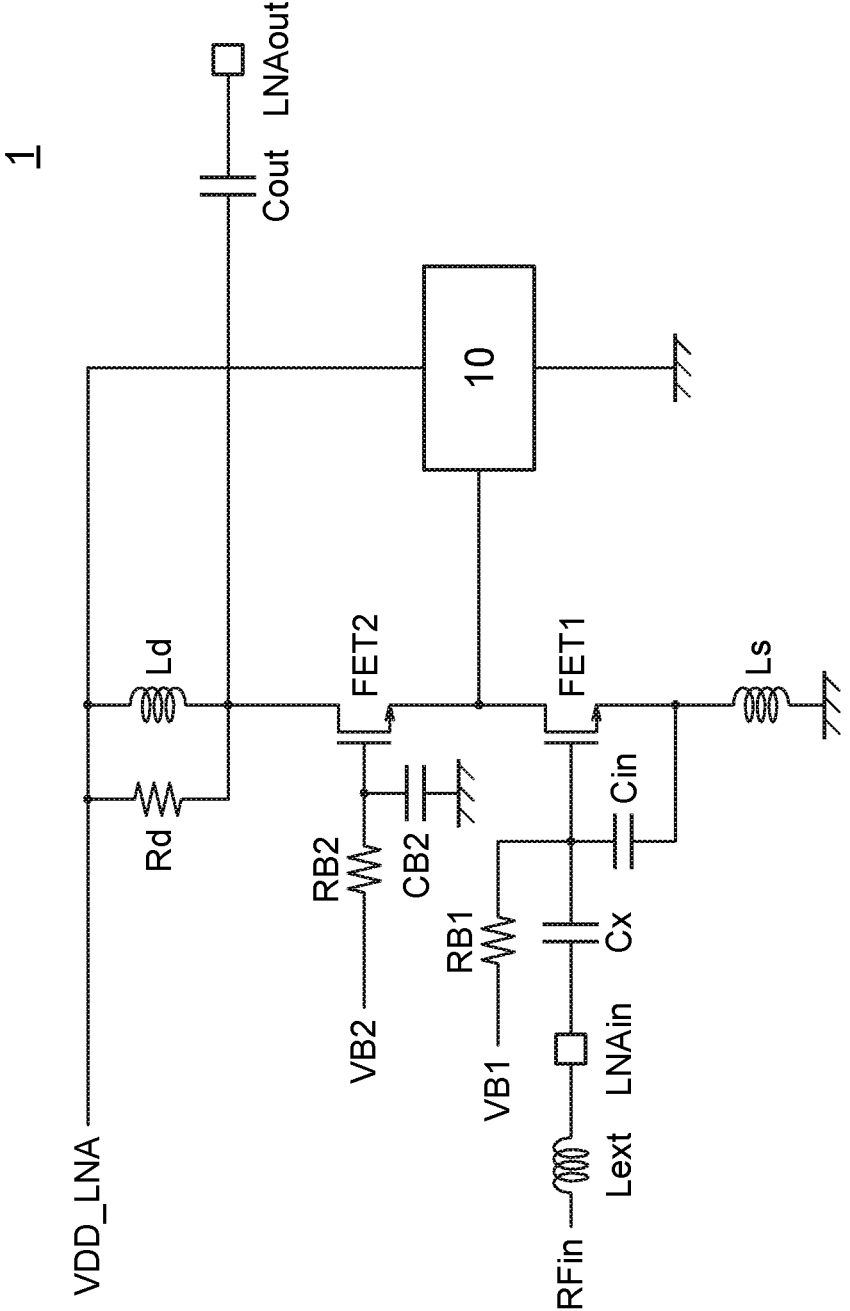


FIG. 1

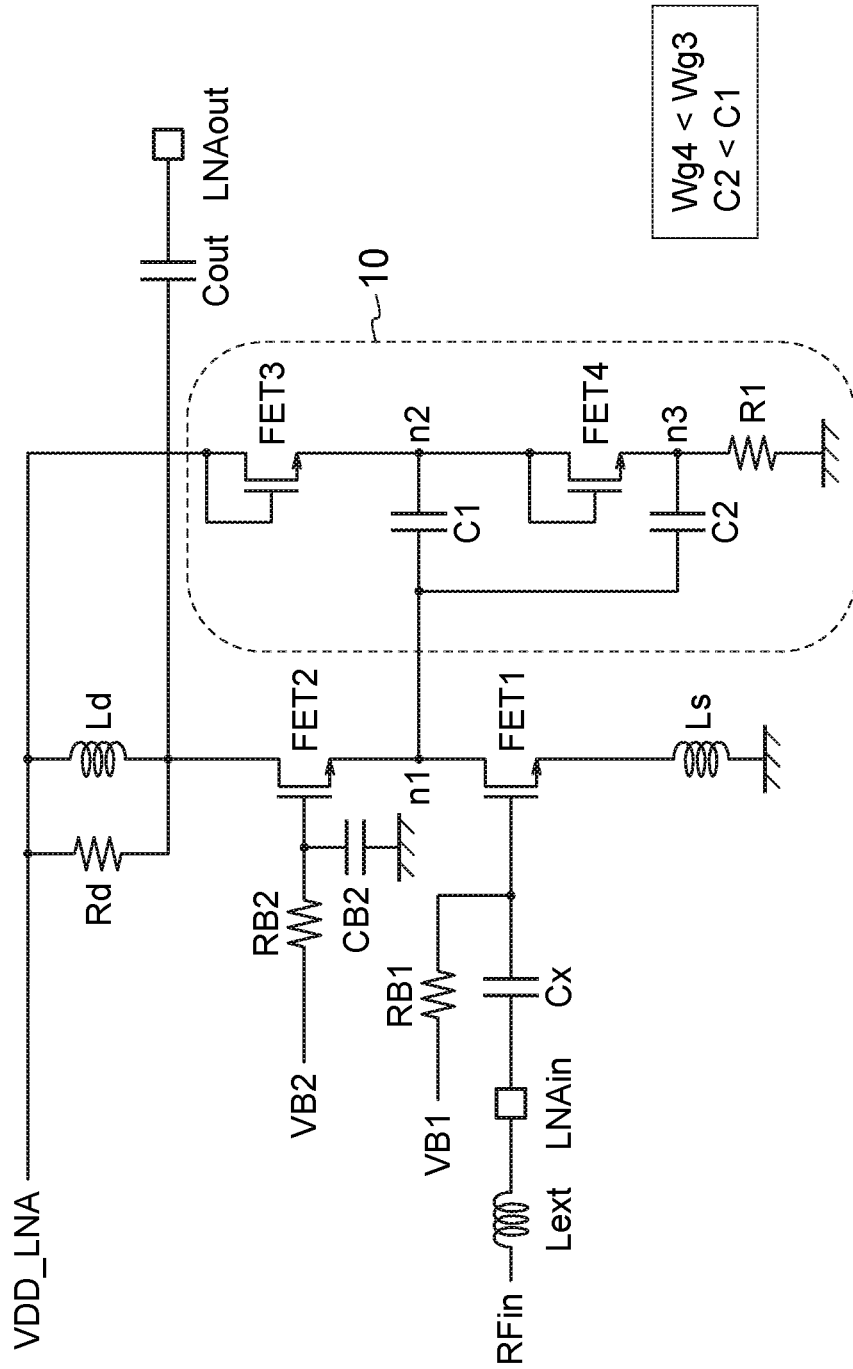
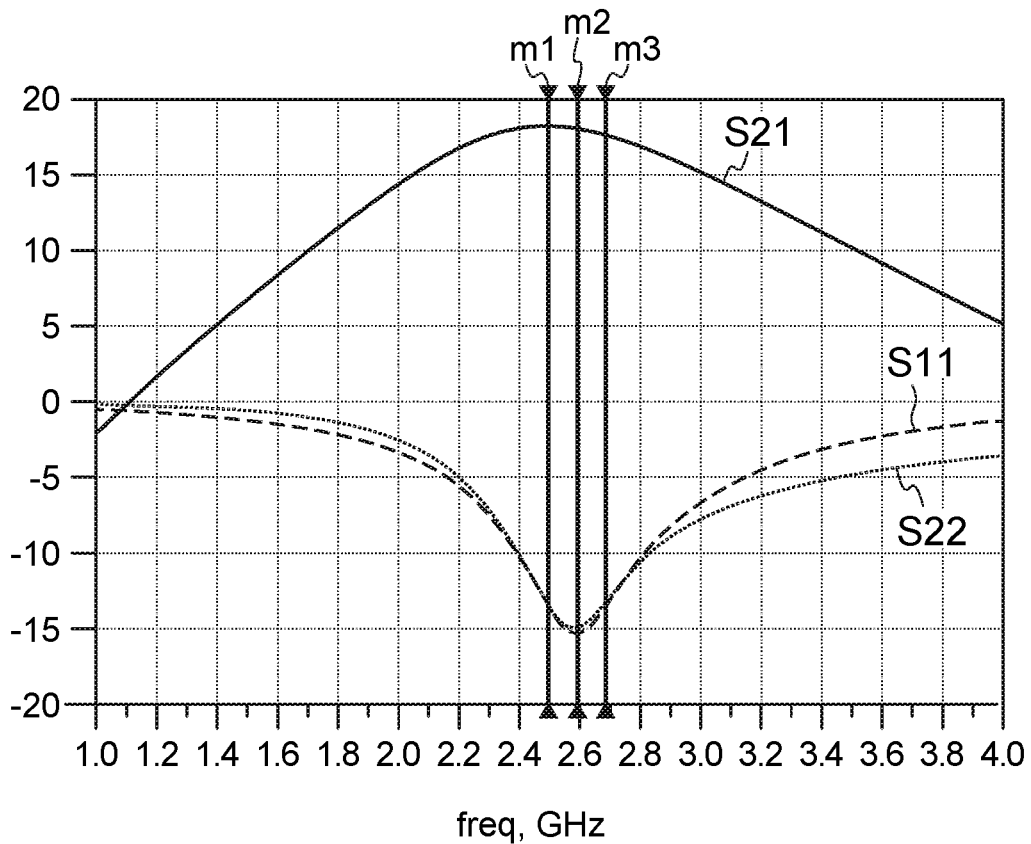


FIG. 2

<p>m1 freq = 2.496GHz dB(S(2,1)) = 18.233 dB(S(1,1)) = -13.430 dB(S(2,2)) = -13.396</p>	<p>m2 freq = 2.593GHz dB(S(2,1)) = 18.056 dB(S(1,1)) = -15.324 dB(S(2,2)) = -14.935</p>	<p>m3 freq = 2.690GHz dB(S(2,1)) = 17.618 dB(S(1,1)) = -13.410 dB(S(2,2)) = -13.111</p>
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dB(S(2,2))
 dB(S(1,1)) - - - - -
 dB(S(2,1)) —————

FIG. 3

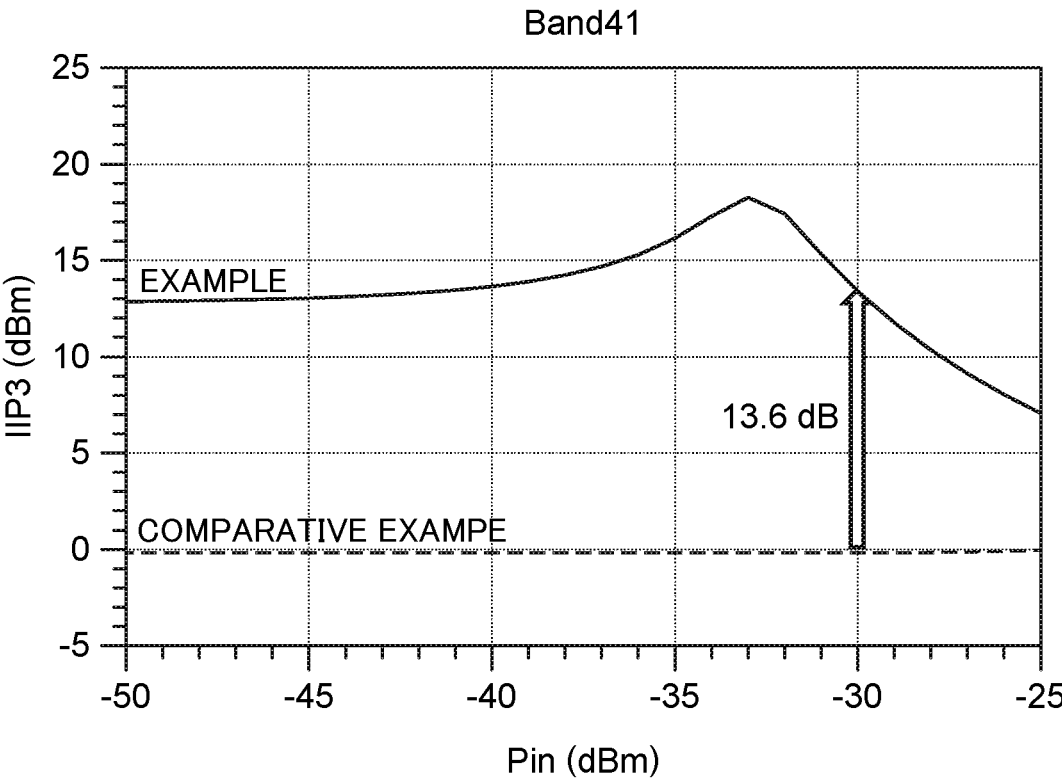


FIG. 4

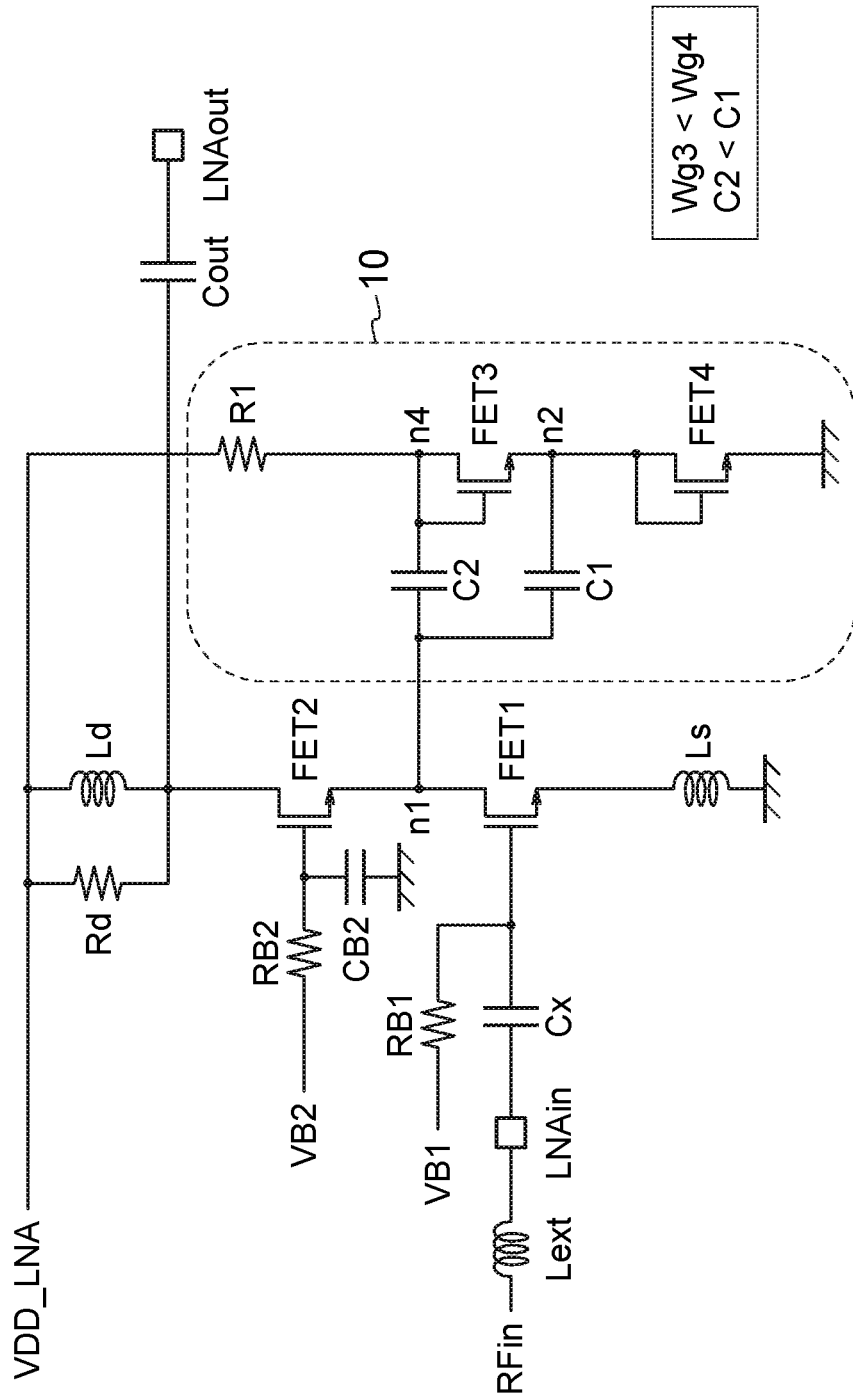
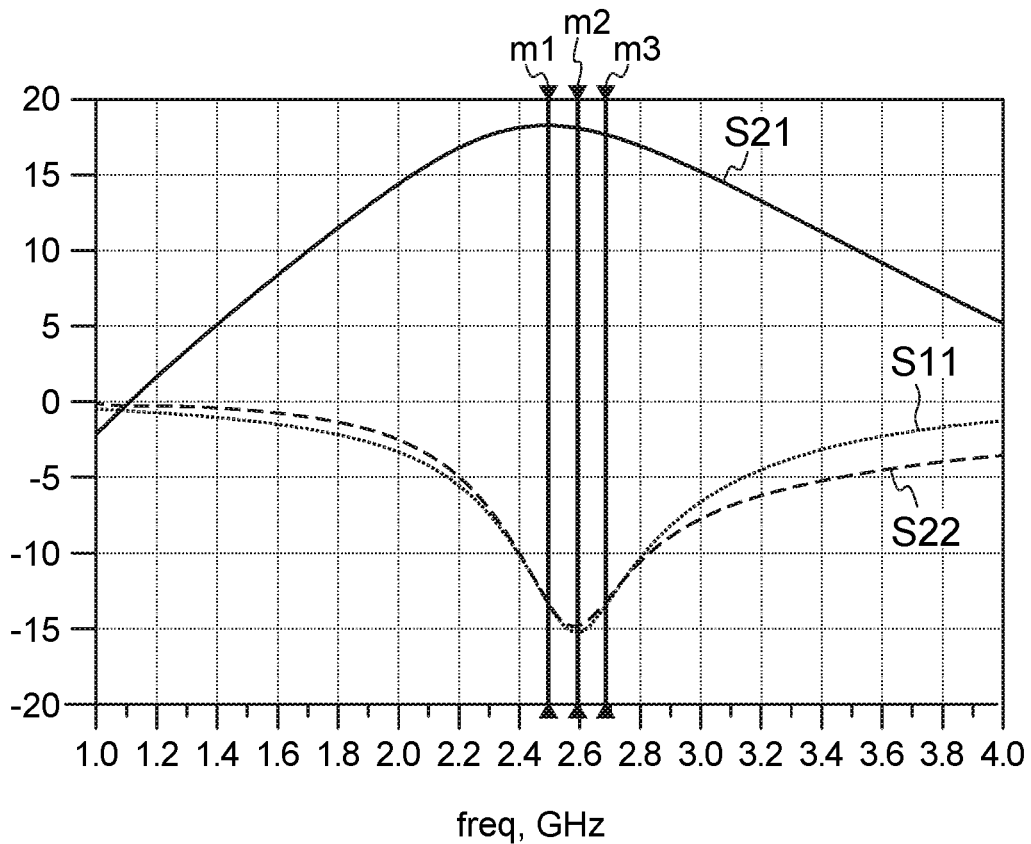


FIG. 5

<p>m1 freq = 2.496GHz dB(S(2,1)) = 18.264 dB(S(1,1)) = -13.388 dB(S(2,2)) = -13.311</p>	<p>m2 freq = 2.593GHz dB(S(2,1)) = 18.087 dB(S(1,1)) = -15.250 dB(S(2,2)) = -14.839</p>	<p>m3 freq = 2.690GHz dB(S(2,1)) = 17.648 dB(S(1,1)) = -13.348 dB(S(2,2)) = -13.056</p>
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dB(S(2,2))
 dB(S(1,1)) - - - - -
 dB(S(2,1)) —————

FIG. 6

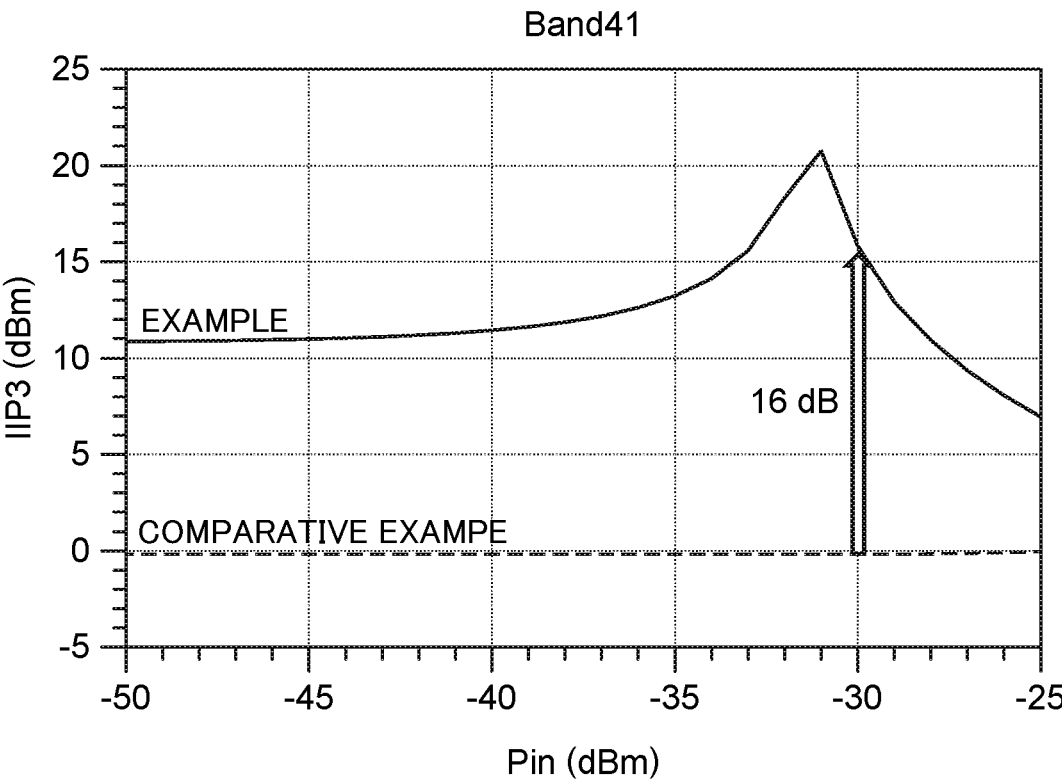


FIG. 7

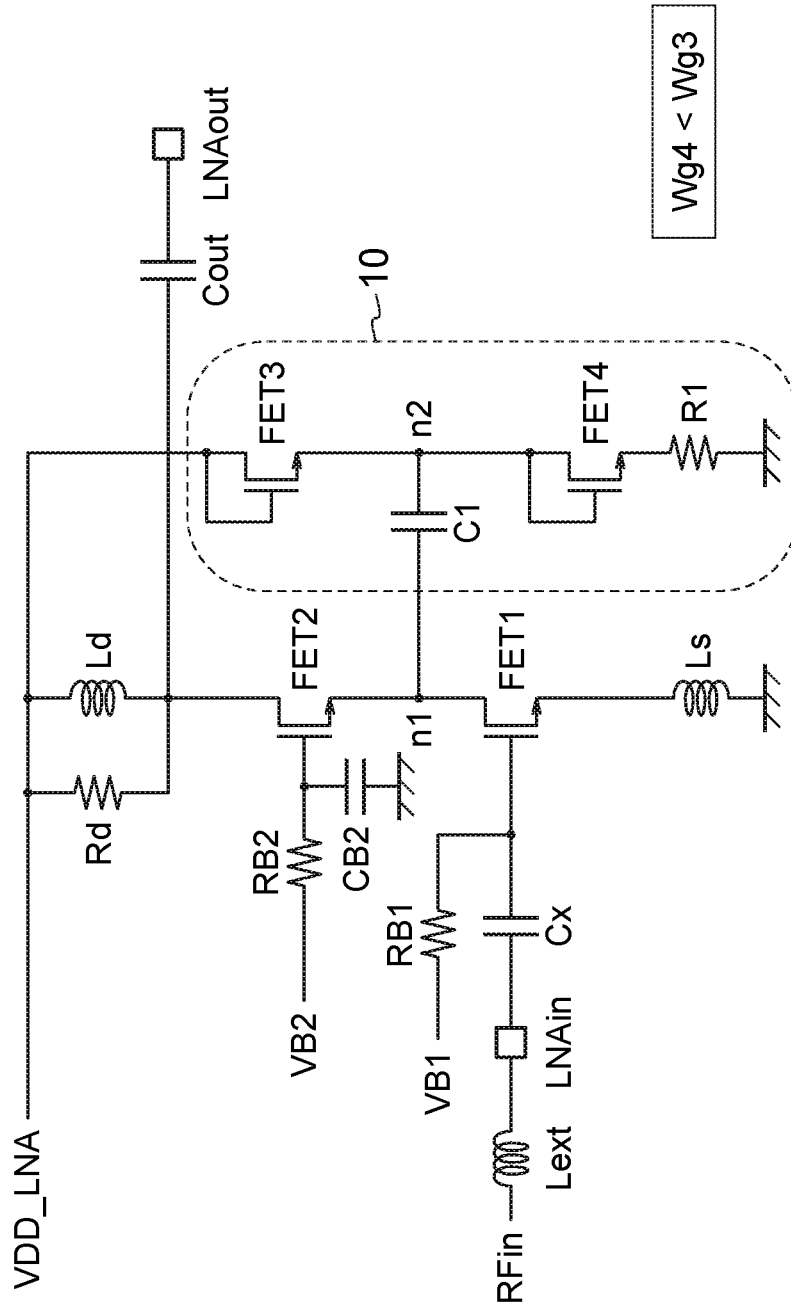
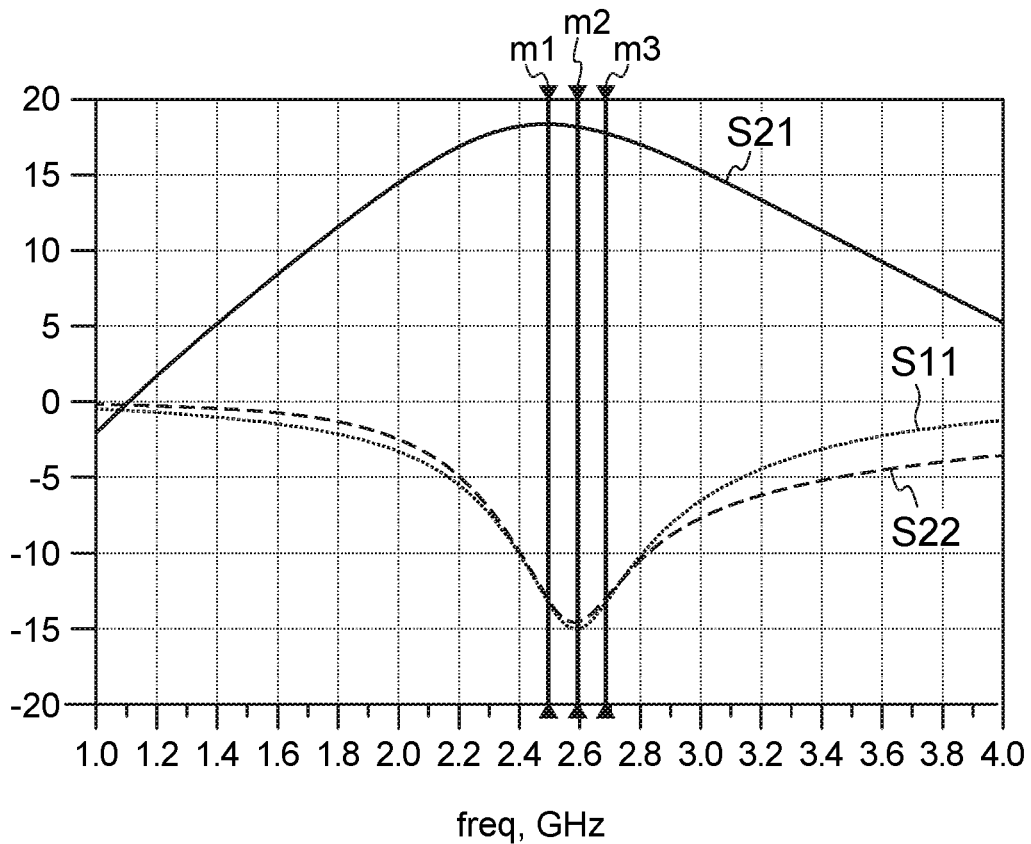


FIG. 8

<p>m1 freq = 2.496GHz dB(S(2,1)) = 18.350 dB(S(1,1)) = -13.282 dB(S(2,2)) = -13.085</p>	<p>m2 freq = 2.593GHz dB(S(2,1)) = 18.172 dB(S(1,1)) = -15.055 dB(S(2,2)) = -14.574</p>	<p>m3 freq = 2.690GHz dB(S(2,1)) = 17.730 dB(S(1,1)) = -13.181 dB(S(2,2)) = -12.893</p>
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dB(S(2,2))
 dB(S(1,1)) - - - - -
 dB(S(2,1)) —————

FIG. 9

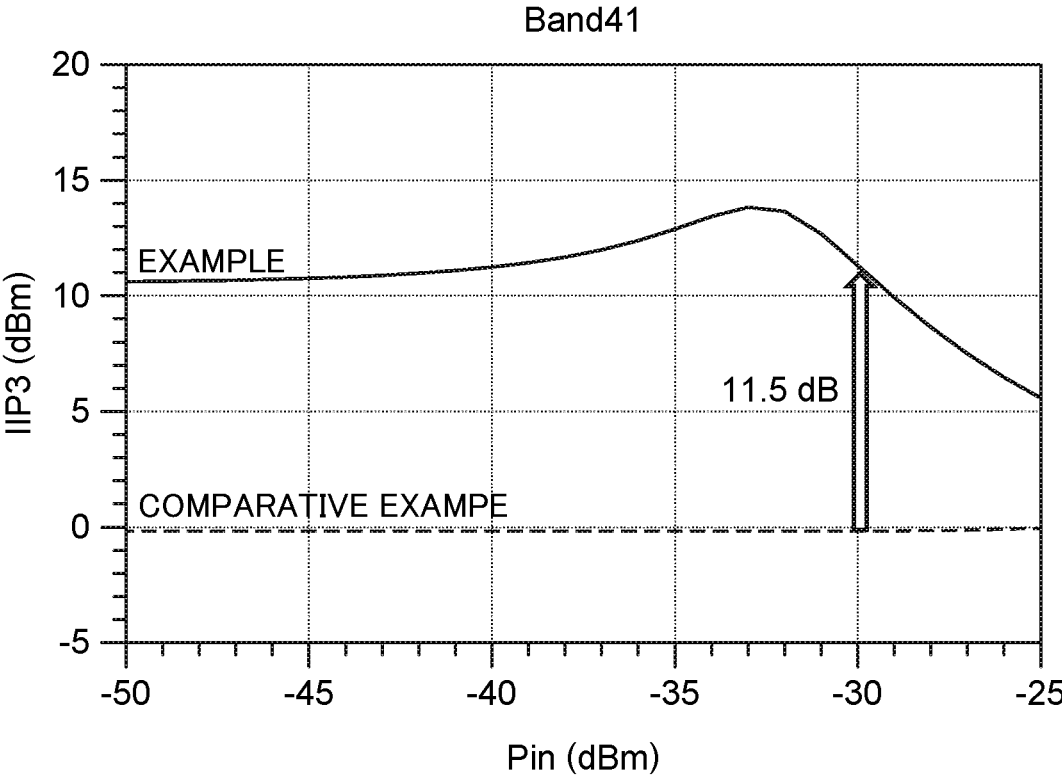


FIG.10

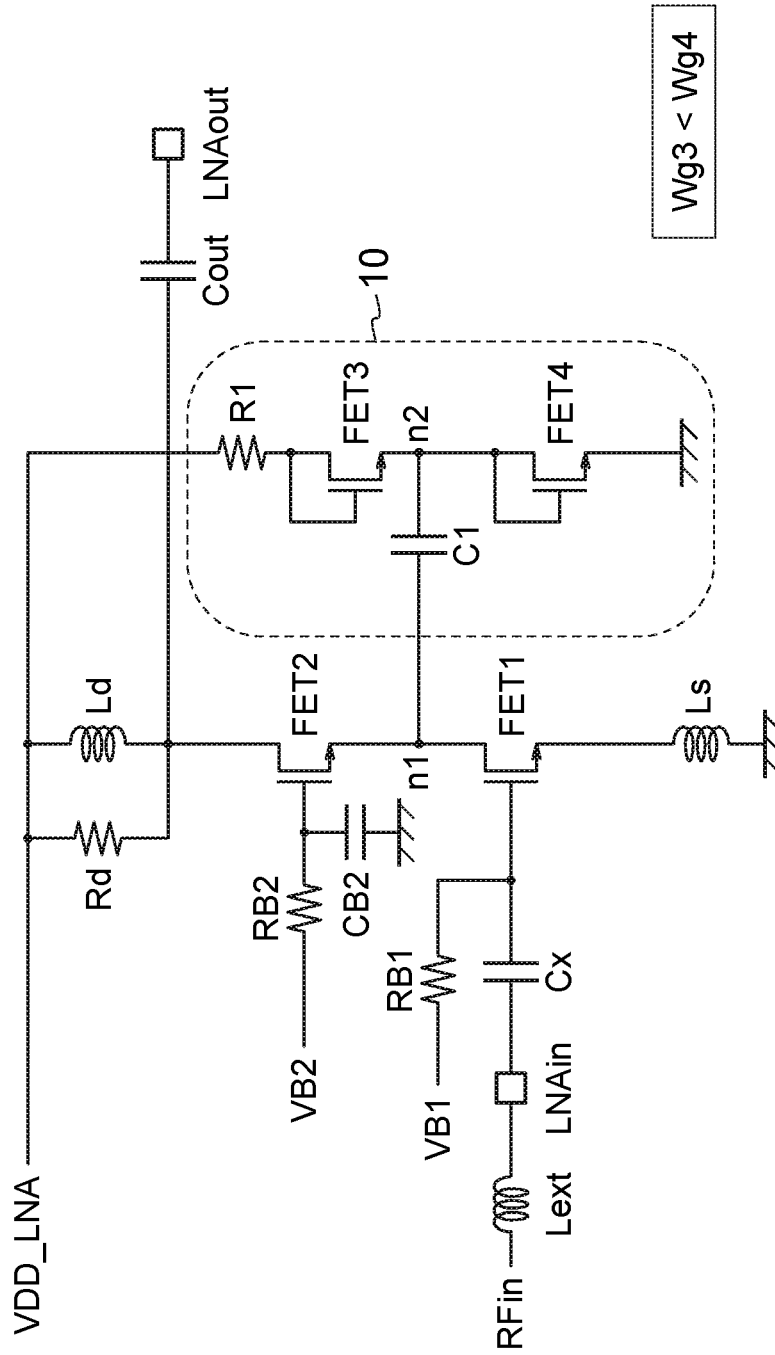
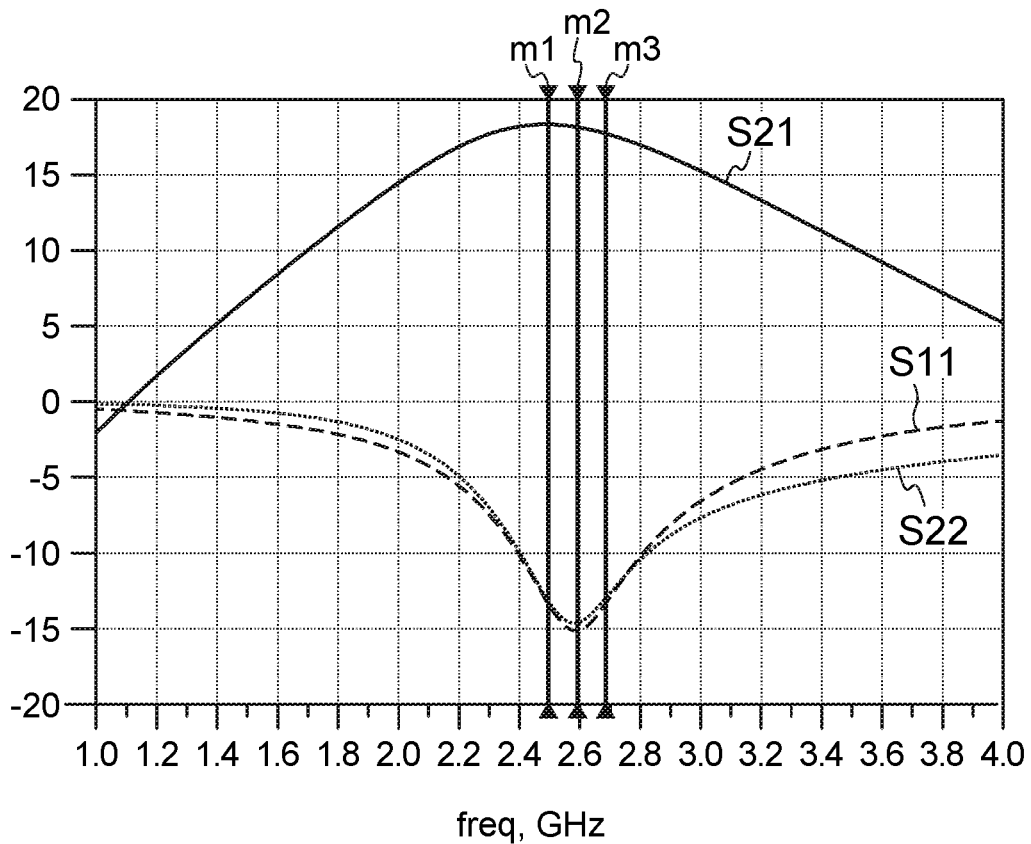


FIG.11

<p>m1 freq = 2.496GHz dB(S(2,1)) = 18.340 dB(S(1,1)) = -13.362 dB(S(2,2)) = -13.160</p>	<p>m2 freq = 2.593GHz dB(S(2,1)) = 18.159 dB(S(1,1)) = -15.138 dB(S(2,2)) = -14.610</p>	<p>m3 freq = 2.690GHz dB(S(2,1)) = 17.714 dB(S(1,1)) = -13.225 dB(S(2,2)) = -12.883</p>
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dB(S(2,2))
 dB(S(1,1)) - - - - -
 dB(S(2,1)) —————

FIG.12

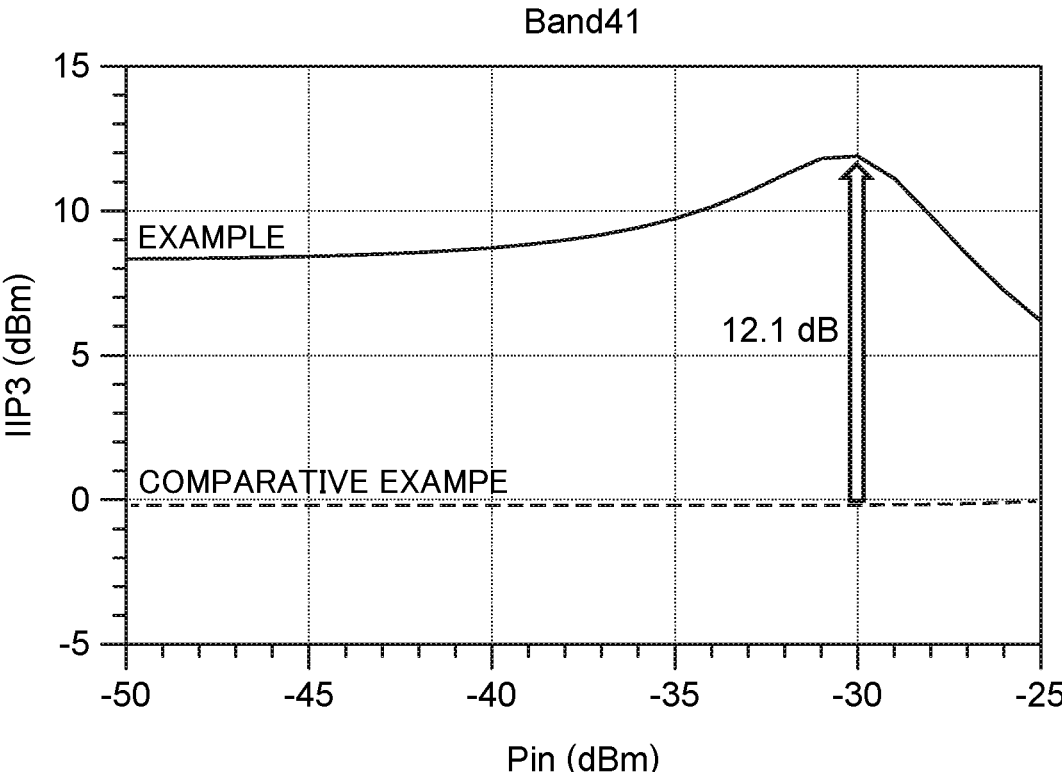


FIG.13

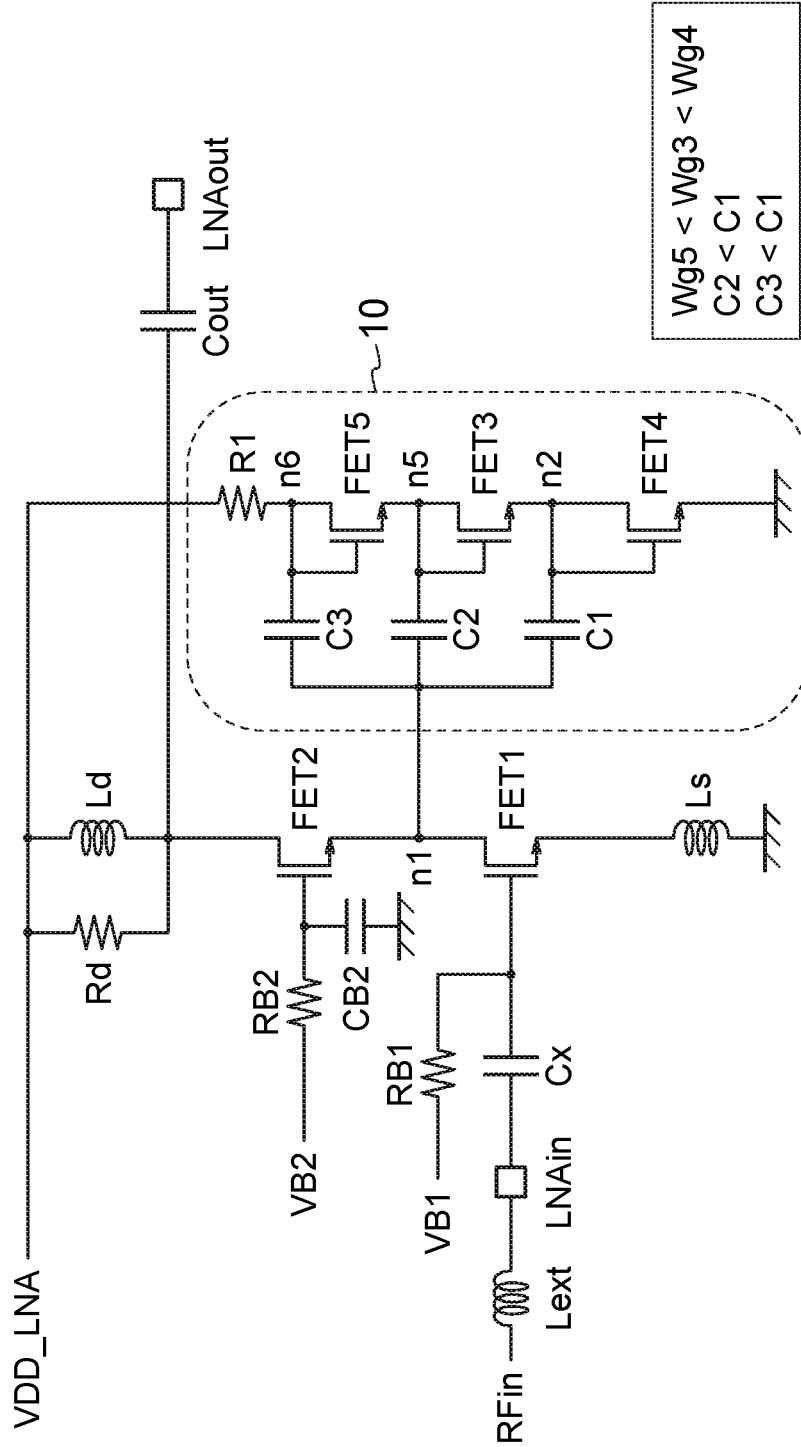
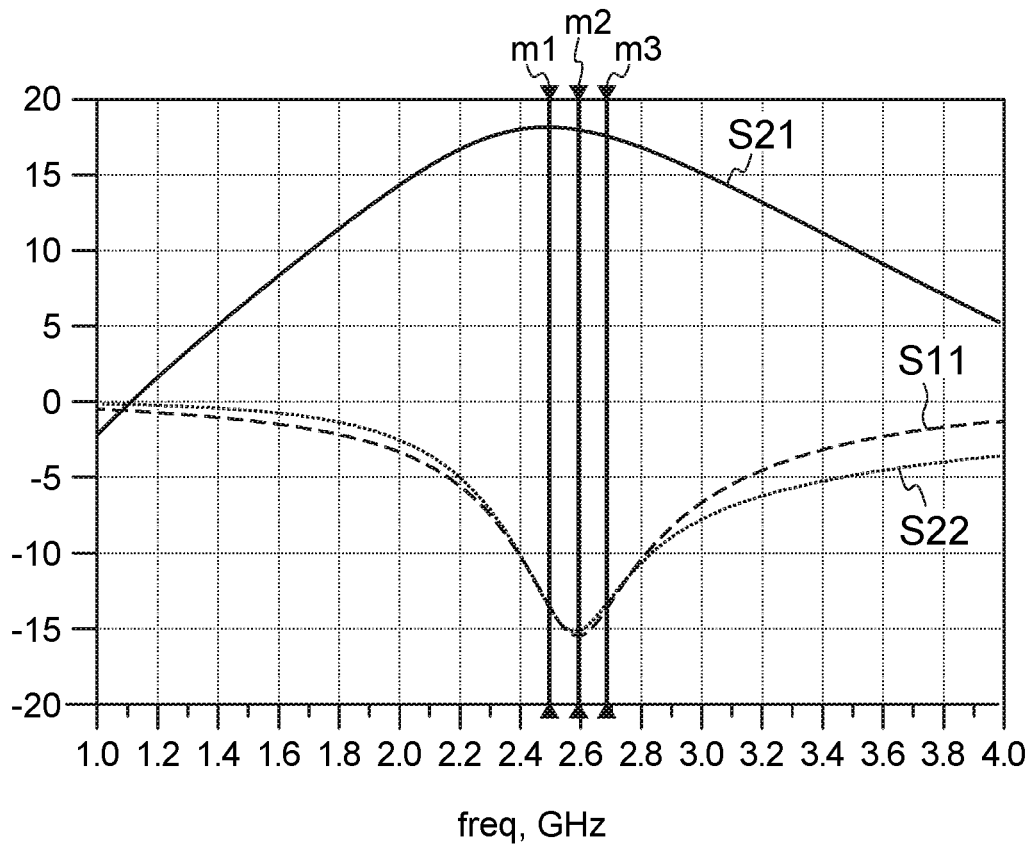


FIG.14

<p>m1 freq = 2.5GHz dB(S(2,1)) = 18.2 dB(S(1,1)) = -13.5 dB(S(2,2)) = -13.6</p>	<p>m2 freq = 2.6GHz dB(S(2,1)) = 18.0 dB(S(1,1)) = -15.5 dB(S(2,2)) = -15.2</p>	<p>m3 freq = 2.7GHz dB(S(2,1)) = 17.5 dB(S(1,1)) = -13.6 dB(S(2,2)) = -13.2</p>
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dB(S(2,2))
 dB(S(1,1)) - - - - -
 dB(S(2,1)) —————

FIG.15

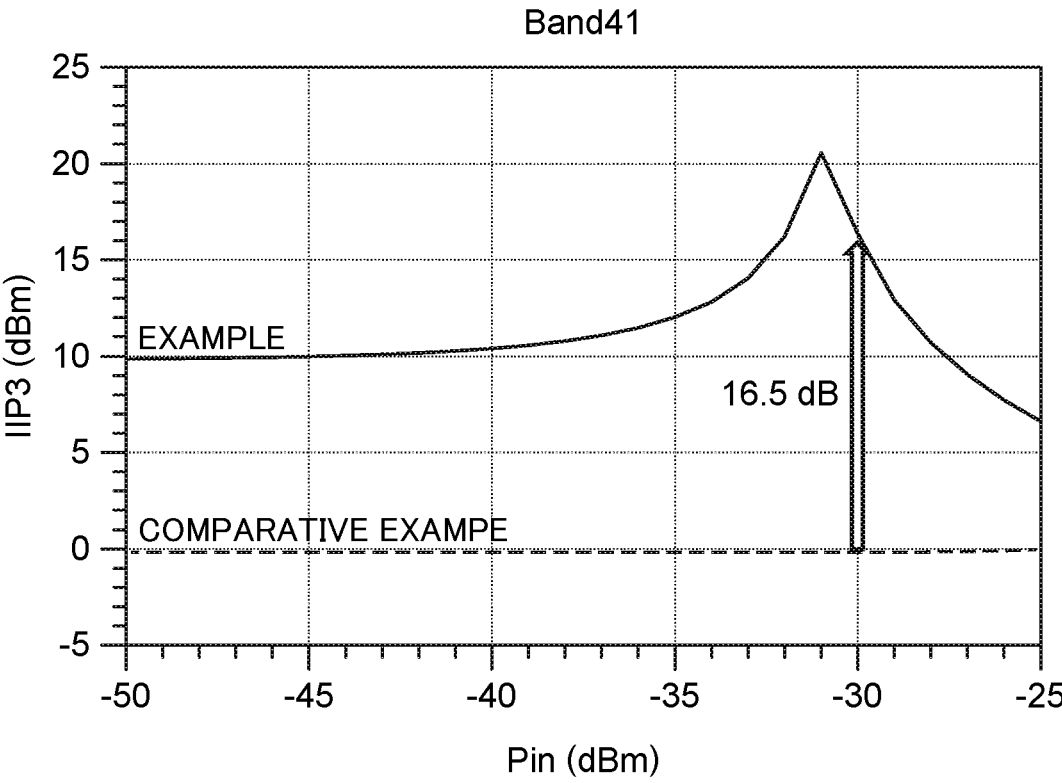


FIG.16

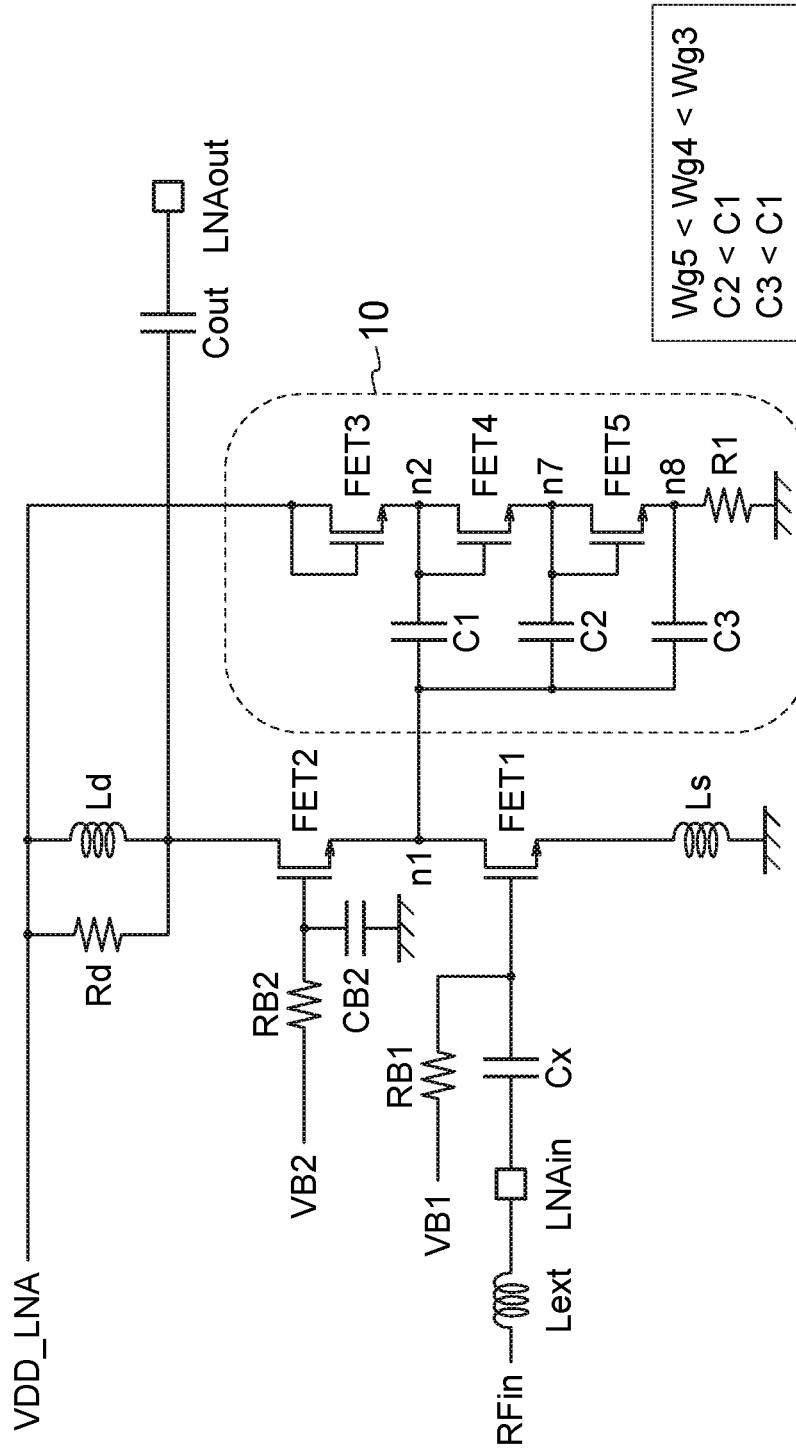
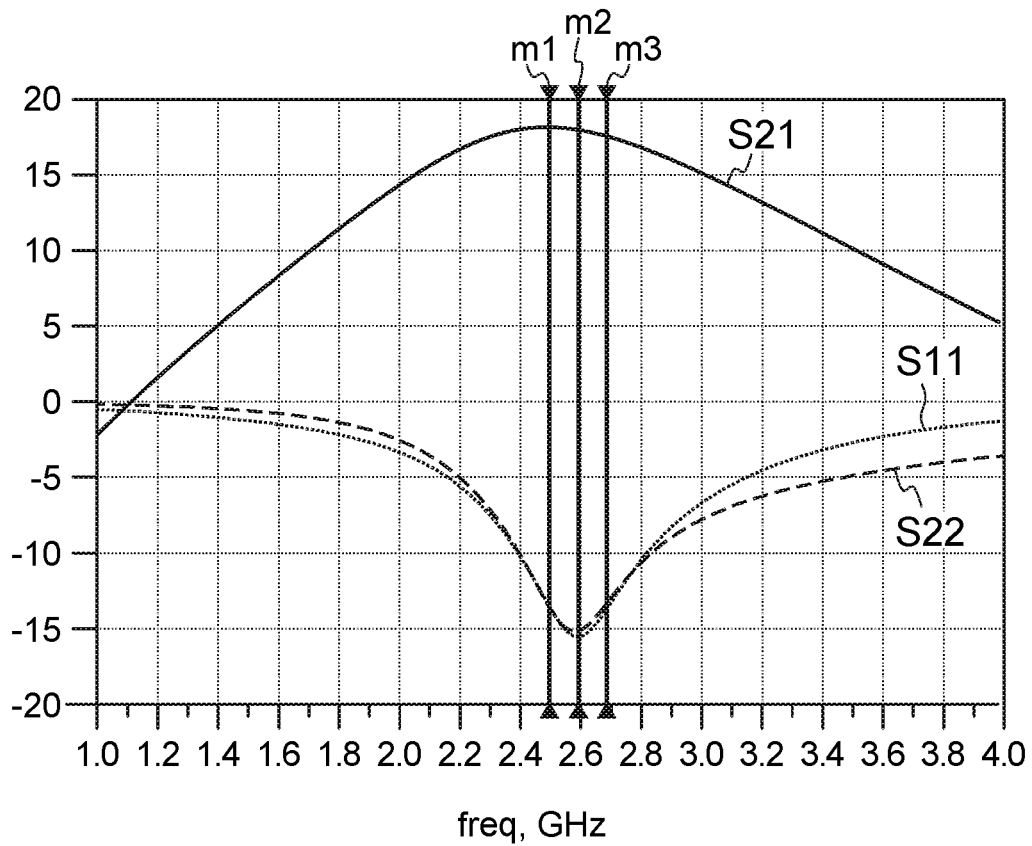


FIG.17

<p>m1 freq = 2.5GHz dB(S(2,1)) = 18.2 dB(S(1,1)) = -13.6 dB(S(2,2)) = -13.6</p>	<p>m2 freq = 2.6GHz dB(S(2,1)) = 18.0 dB(S(1,1)) = -15.5 dB(S(2,2)) = -15.1</p>	<p>m3 freq = 2.7GHz dB(S(2,1)) = 17.6 dB(S(1,1)) = -13.5 dB(S(2,2)) = -13.2</p>
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dB(S(2,2))
 dB(S(1,1)) - - - - -
 dB(S(2,1)) —————

FIG.18

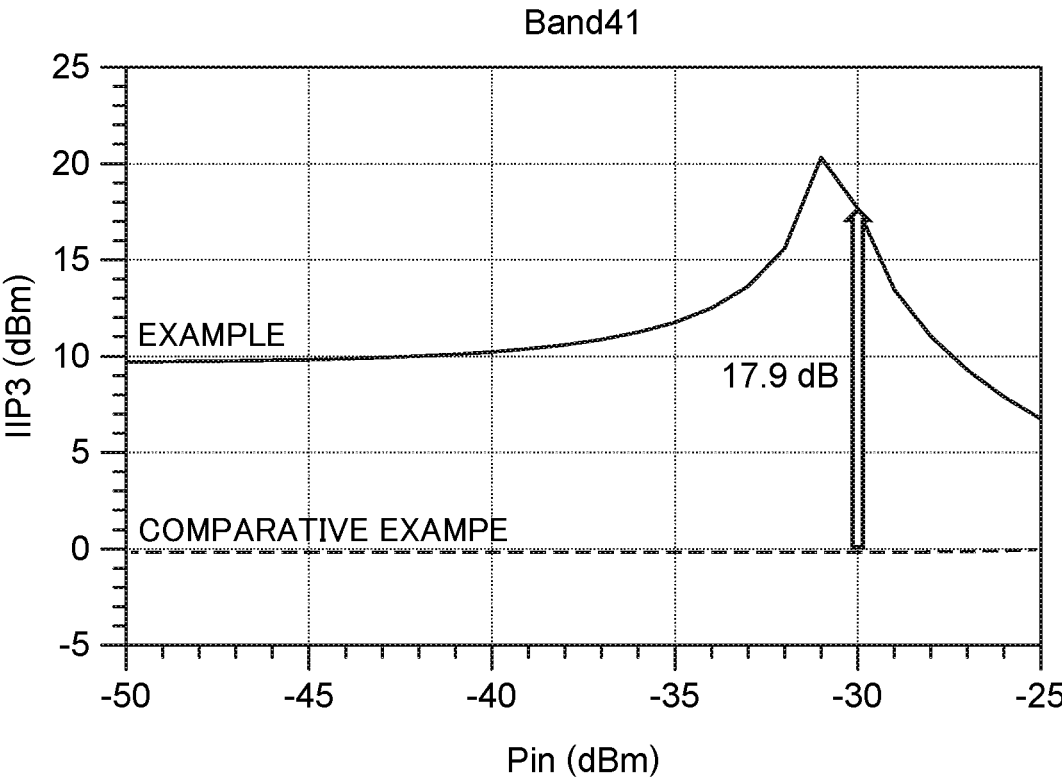


FIG.19

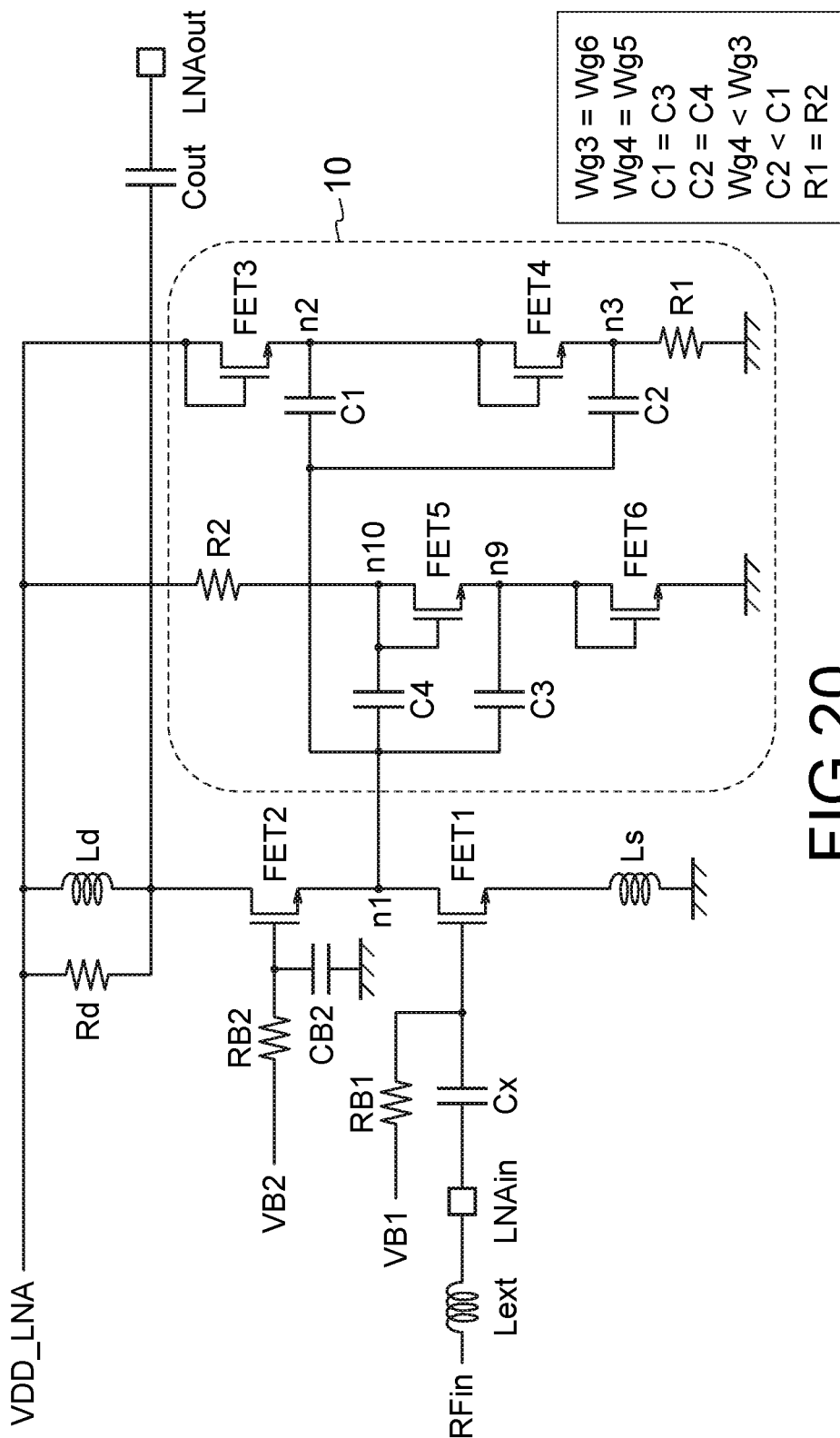
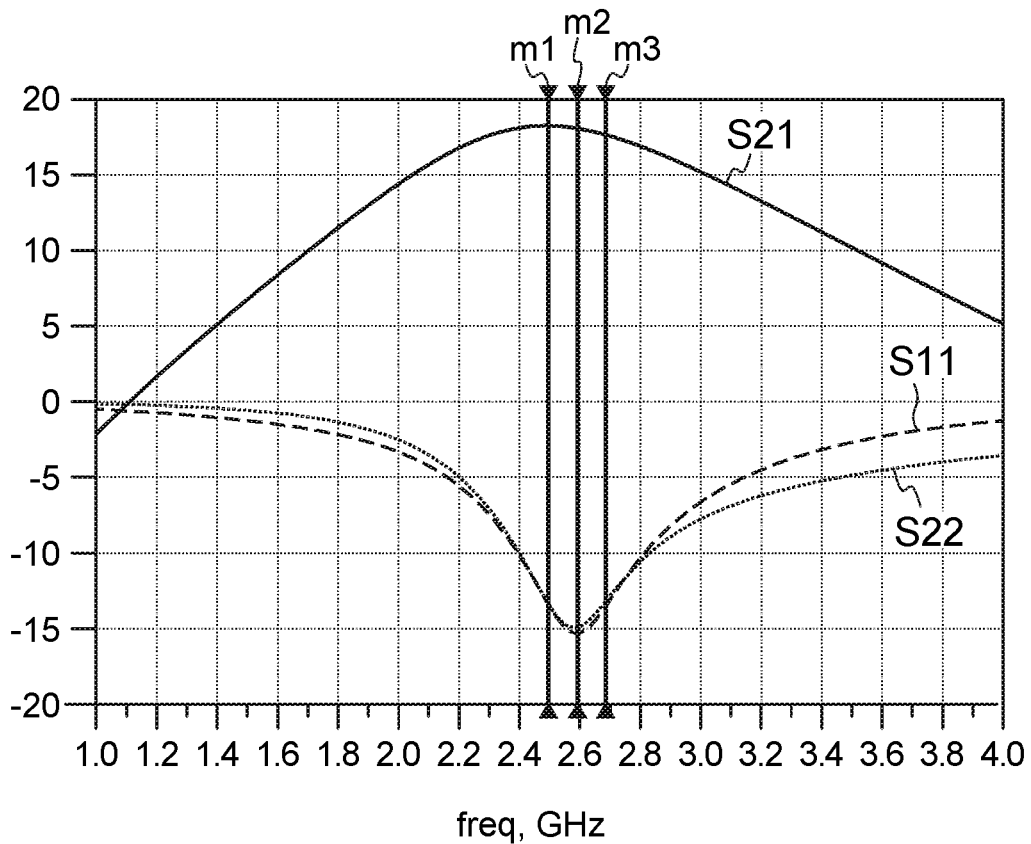


FIG. 20

m1 freq = 2.496GHz dB(S(2,1)) = 18.249 dB(S(1,1)) = -13.425 dB(S(2,2)) = -13.365	m2 freq = 2.593GHz dB(S(2,1)) = 18.071 dB(S(1,1)) = -15.301 dB(S(2,2)) = 14.888	m3 freq = 2.690GHz dB(S(2,1)) = 17.632 dB(S(1,1)) = -13.384 dB(S(2,2)) = -13.076
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dB(S(2,2))
 dB(S(1,1)) - - - - -
 dB(S(2,1)) —————

FIG.21

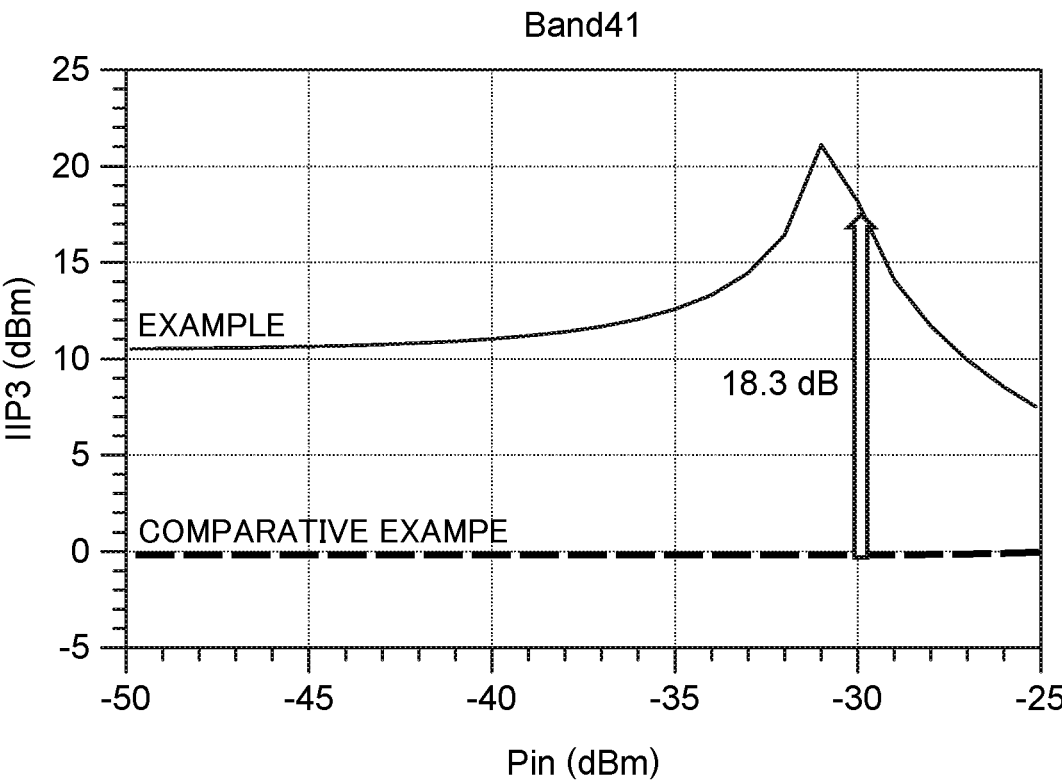


FIG.22

HIGH-FREQUENCY AMPLIFIER CIRCUITRY AND SEMICONDUCTOR DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2019-020723, filed on Feb. 7, 2019, the entire contents of which are incorporated herein by reference.

FIELD

[0002] The embodiment of the present invention relate to high-frequency amplifier circuitry and a semiconductor device.

BACKGROUND

[0003] For a Low Noise Amplifier (LNA), generally, a SiGe bipolar process is used, and the one made by a CMOS process on a Silicon On Insulator (SOI) substrate increases recently. This is because a high functional circuit can be realized by incorporating a high-frequency switch FET in the LNA. In recent years, Carrier Aggregation (CA) is introduced to speed up the radio communication. To cope with the carrier aggregation, there is a growing demand for Third Order Input Intercept Point (IIP3) recently.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a diagram illustrating an LNA according to an embodiment;
 [0005] FIG. 2 is a diagram illustrating an LNA according to one embodiment;
 [0006] FIG. 3 is a chart illustrating an S parameter of the circuit in FIG. 2;
 [0007] FIG. 4 is a chart illustrating an IIP3 of the circuit in FIG. 2; FIG. 5 is a diagram illustrating an LNA according to one embodiment;
 [0008] FIG. 6 is a chart illustrating an S parameter of the circuit in FIG. 5;
 [0009] FIG. 7 is a chart illustrating an IIP3 of the circuit in FIG. 5;
 [0010] FIG. 8 is a diagram illustrating an LNA according to one embodiment;
 [0011] FIG. 9 is a chart illustrating an S parameter of the circuit in FIG. 8;
 [0012] FIG. 10 is a chart illustrating an IIP3 of the circuit in FIG. 8;
 [0013] FIG. 11 is a diagram illustrating an LNA according to one embodiment;
 [0014] FIG. 12 is a chart illustrating an S parameter of the circuit in FIG. 11;
 [0015] FIG. 13 is a chart illustrating an IIP3 of the circuit in FIG. 11;
 [0016] FIG. 14 is a diagram illustrating an LNA according to one embodiment;
 [0017] FIG. 15 is a chart illustrating an S parameter of the circuit in FIG. 14;
 [0018] FIG. 16 is a chart illustrating an IIP3 of the circuit in FIG. 14;
 [0019] FIG. 17 is a diagram illustrating an LNA according to one embodiment;
 [0020] FIG. 18 is a chart illustrating an S parameter of the circuit in FIG. 17;

[0021] FIG. 19 is a chart illustrating an IIP3 of the circuit in FIG. 17;

[0022] FIG. 20 is a diagram illustrating an LNA according to one embodiment;

[0023] FIG. 21 is a chart illustrating an S parameter of the circuit in FIG. 20; and

[0024] FIG. 22 is a chart illustrating an IIP3 of the circuit in FIG. 20.

DETAILED DESCRIPTION

[0025] According to one embodiment, a high-frequency amplifier circuitry includes an amplifier circuit and a distortion compensation circuit. The amplifier circuit includes a first transistor, an inductor, and a second transistor. The first transistor has a gate to which an input signal is applied. The inductor has one terminal which is connected to a source of the first transistor and another terminal which is grounded. The second transistor has a source which is connected to a drain of the first transistor, a gate which is grounded, and a drain which is connected to a power supply voltage terminal, and is configured to output from the drain a signal obtained by amplifying the input signal. The distortion compensation circuit includes a third transistor, a fourth transistor, and a first capacitor. The third transistor has a drain and a gate which are connected to each other, the third transistor connected to the power supply voltage terminal on the drain side. The fourth transistor has a drain and a gate which are connected to a source of the third transistor, and is grounded on a source side. The first capacitor connects nodes between the drain of the first transistor and the source of the second transistor, and, the source of the third transistor.

[0026] Embodiments will now be explained with reference to the drawings. Note that though the embodiments are explained and illustrated with some components omitted, modified or simplified in this specification and the attached drawings for convenience of easy understanding and illustration, the technical contents at the level in which the same functions can be expected will be interpreted while being included in the embodiments. Further, in the drawings attached to this specification, the scale and the aspect ratio and so on are changed from the original size and exaggerated for convenience of illustration and easy understanding.

[0027] FIG. 1 is a diagram illustrating a configuration of an LNA to be explained in this specification. An LNA1 includes: an amplifier circuit having a grounded-source first transistor FET1 and a grounded-gate second transistor FET2 which are cascode-connected; and an IIP3 compensation circuit (distortion compensation circuit) 10. The amplifier circuit may include capacitors C_x, C_{in} and a source inductor L_s as input matching elements, and may include a capacitor C_{out}, a resistor R_d, and an inductor L_d as output matching elements. The amplifier circuit may further include resistors RB1, RB2 to prevent a high-frequency signal from flowing to a bias potential generation circuit.

[0028] The first transistor FET1 includes the source inductor L_s between its source and a ground point, and functions as a grounded-source transistor having inductive source degeneration. The capacitor C_x is connected between the gate of the first transistor FET1 and an input terminal LNA_{in}, and the capacitor C_{in} is connected between the gate and the source.

[0029] The second transistor FET2 has a gate to which a capacitor CB2 is connected, and functions (in a high-

frequency manner) as a grounded-gate transistor. The second transistor FET2 has a source connected to the drain of the first transistor FET1 and a drain connected to an output port via an output matching circuit, and amplifies the high-frequency signal inputted from the drain of the first transistor FET1 and outputs the amplified signal.

[0030] The source inductor L_s , the capacitors C_x , C_{in} , and an external inductor L_{ext} provided in the external part of the LNA1 function as the input matching elements. The input matching elements achieve desired impedance matching taking gain matching and noise matching of an amplifying transistor into account. The capacitor C_x also serves as a function of blocking a direct-current component. Besides, the capacitor C_{in} is not always a necessary component, and becomes an unnecessary component, for example, depending on a frequency band. The capacitor C_{in} is omitted in the following explanation, but the same explanation is applicable to a configuration including the capacitor C_{in} .

[0031] An amplifier circuit including the first transistor FET1, the second transistor FET2, and the source inductor L_s is formed. The amplifier circuit may further include the following circuit elements.

[0032] Between the drain of the second transistor FET2 and a power supply node VDD_LNA (power supply voltage terminal or an output of an internal voltage regulator), the inductor L_d is connected, and the resistor R_d is connected in parallel with the L_d . Between the drain of the second transistor FET2 and an output terminal LNAout, the capacitor C_{out} is connected. The inductor L_d , the resistor R_d , and the capacitor C_{out} form the output matching circuit. The resistor R_d is provided for gain adjustment and stabilization.

[0033] From the not-illustrated bias potential generation circuit, a bias potential VB1 to the gate of the first transistor FET1, a bias potential VB2 to the gate of the second transistor FET2, and a bias potential VDD_LNA to the drain of the second transistor FET2 are supplied. Note that the resistors RB1, RB2 are provided to prevent the high-frequency signal from being transmitted to the bias potential generation circuit.

[0034] The IIP3 compensation circuit 10 is a distortion compensation circuit provided to realize distortion compensation of the LNA1, in particular, excellent IIP3 characteristics for the amplifier circuit which amplifies the input signal and outputs the amplified signal. The IIP3 compensation circuit (distortion compensation circuit) is connected to the power supply node VDD_LNA being an output of an internal voltage regulator and to a node between the drain of the first transistor FET1 and the source of the second transistor FET2. The IIP3 compensation circuit 10 generates reverse distortion with respect to the distortion of the signal generated in the LNA1 and compensate the distortion to thereby improve the IIP3. For example, the IIP3 compensation circuit 10 is provided with a transistor and a capacitor to generate third-order intermodulation distortion having reverse characteristics to those of third-order intermodulation distortion generated in the case where the IIP3 compensation circuit 10 is not provided. Hereinafter, embodiments of the IIP3 compensation circuit 10 will be explained. The detailed operation of the LNA1 will be omitted.

[0035] As explained above, the LNA1 according to the embodiments explained below includes an amplifier circuit, and an IIP3 compensation circuit (distortion compensation circuit) connected to the amplifier circuit. The IIP3 compensation circuit (distortion compensation circuit) includes

at least a third transistor which has a drain and a gate connected to each other and is connected to a power supply voltage terminal on a drain side, a fourth transistor which has a drain and a gate connected to the source of the third transistor and is grounded on a source side, and a first capacitor which connects a node between the transistors of the amplifier circuit and the source of the third transistor.

[0036] Note that each matching circuit element is illustrated as an example, and is not an essential point in the embodiments explained below. In other words, the output matching circuit element may have another configuration and may be provided outside the LNA1 in a broad sense.

[0037] The relationship with the gate width of the transistor will be illustrated together with a circuit diagram. Wg indicates the gate width and is given the same index as that of the corresponding transistor to indicate which transistor has the gate width. For example, the gate width of the third transistor FET3 is described as Wg3, and the gate width of the fourth transistor FET4 is described as Wg4. The same applies to the drawings. The electrostatic capacitance of a capacitor is replaced, for description, by the name of the capacitor. For example, the electrostatic capacitance of a capacitor C1 is simply described as C1. The resistance value is similarly replaced, for description, by the name of the resistor.

First Embodiment

[0038] FIG. 2 is a diagram illustrating an LNA1 according to this embodiment. In the LNA1 according to this embodiment, an IIP3 compensation circuit (distortion compensation circuit) 10 includes a third transistor FET3, a fourth transistor FET4, and a first resistor R1 which are connected in series between a power supply node VDD_LNA being an output of an internal voltage regulator and the ground point, and further includes a first capacitor C1 and a second capacitor C2.

[0039] The third transistor FET3 has a drain and a gate connected to each other, and the drain and the gate are connected to the power supply node VDD_LNA. The fourth transistor FET4 has a drain and a gate connected to each other, and the drain and the gate are connected to the source of the third transistor FET3. The first resistor R1 has one terminal connected to a source of the fourth transistor FET4 and is grounded at another terminal. In other words, the fourth transistor FET4 has the source grounded via the first resistor R1.

[0040] The capacitor C1 connects a first node n1 between a drain of a first transistor FET1 and a source of a second transistor FET2 and a second node n2 between the source of the third transistor FET3 and the drain of the fourth transistor FET4. The second capacitor C2 connects the first node n1 and a third node n3 between the source of the fourth transistor FET4 and the first resistor R1.

[0041] In this embodiment, the gate widths of the third transistor FET3 and the fourth transistor FET4 satisfy $Wg4 < Wg3$, and the electrostatic capacitances thereof satisfy $C2 < C1$.

[0042] For example, regarding each transistor, the gate oxide film thickness is 2.5 nm, the gate length is 0.14 μm , the threshold voltage is 0.37 V, Wg1 and Wg2 are 300 nm, Wg3 is 15 μm , Wg4 is 5 μm , R1 is 4.1 k Ω , C1 is 0.34 pF, and C2 is 0.12 pF.

[0043] FIG. 3 is a chart illustrating Scattering Parameter (S parameter) being input/output characteristics in the case

where a high-frequency input node RFin is a port 1 and an output port LNAout is a port 2 in the case of the aforementioned circuit constants. A solid line indicates S21, a broken line indicates S11, and a dotted line indicates S22. m1 illustrated in the chart indicates observation at a frequency of 2496 MHz, m2 indicates observation at a frequency of 2593 MHz, and m3 indicates observation at a frequency of 2690 MHz. The same applies to the explanation in the following embodiments.

[0044] The degree of amplification of the output signal to the input signal can be represented by S21. A larger S21 indicates a higher gain in a focused frequency band (for example, Band41: 2496 MHz to 2690 MHz). The degree of reflection (reflection property) on the port on the input side with respect to the input signal is represented by S11, and is desired to be low (for example, -10 dB or lower) because impedance match is required in principle at the input/output port in the high-frequency circuit. The same applies to S22 on the output side.

[0045] As illustrated in the chart, it is found that the curve of S21 takes a high value in a focused frequency range. On the other hand, curves of S11 and S22 take low values in the focused frequency range.

[0046] Numerical values indicated at the upper part in the chart represent numerical values of parameters at the respective observation points. The gain at the center of the range is excellent such as 18.06 dB, and both S11 and S22 in the range are -13 dB or lower and satisfy the general requirement (-12 dB or lower). In this embodiment, a bias current Idd_Ina is 6.138 mA which is large by the bias current (171 uA) in the IIP3 compensation circuit (distortion compensation circuit) 10 as compared with the case where the IIP3 compensation circuit (distortion compensation circuit) 10 in FIG. 1 is not provided. Hereinafter, a circuit in which the IIP3 compensation circuit (distortion compensation circuit) 10 in FIG. 1 is not provided is described as a comparative example. The S parameter and Noise Figure (NF) according to this embodiment are substantially the same as the S parameter and noise characteristics in the comparative example.

[0047] FIG. 4 is a chart illustrating Pin dependence of the IIP3 according to this embodiment. The IIP3 when the power level of the input signal is -30 dBm is 13.4 dBm which is improved by 13.6 dB as compared with the comparative example.

[0048] As explained above, according to this embodiment, provision of the distortion compensation circuit enables realization of the LNA excellent in IIP3. The distortion compensation circuit includes the diode-connected transistors and the resistor which are connected in series, and the capacitors connecting the nodes between the transistors and between the transistor and the resistor to the node between the cascode-connected transistors constituting the amplifier circuit, thereby suppressing the three-dimensional distortion. The distortion compensation circuit according to this embodiment can be mounted on an SOI, and therefore can achieve downsizing and reduction in power consumption.

Second Embodiment

[0049] FIG. 5 is a diagram illustrating an LNA1 according to a second embodiment. In the LNA1 according to this embodiment, an IIP3 compensation circuit 10 includes a first resistor R1, a third transistor FET3, and a fourth transistor FET4 which are connected in series between a power supply

node VDD_LNA being an output of an internal voltage regulator and the ground point, and further includes a first capacitor C1 and a second capacitor C2.

[0050] The first resistor R1 has one terminal connected to the power supply node VDD_LNA. The third transistor FET3 has a drain and a gate connected to each other, and the drain and the gate are connected to another terminal of the first resistor R1. In other words, the third transistor FET3 has the drain and the gate connected to the power supply node VDD_LNA via the first resistor R1. The fourth transistor FET4 has a drain and a gate connected to each other, and the drain and the gate are connected to a source of the third transistor FET3, and the fourth transistor FET4 has a source which is grounded.

[0051] The capacitor C1 connects the first node n1 and the second node n2. The second capacitor C2 connects the first node n1 and a fourth node n4 between the drain of the third transistor FET3 and the first resistor R1.

[0052] In this embodiment, the gate widths of the third transistor FET3 and the fourth transistor FET4 satisfy $Wg3 < Wg4$, and the electrostatic capacitances thereof satisfy $C2 < C1$.

[0053] For example, regarding each transistor, the gate oxide film thickness is 2.5 nm, the gate length is 0.14 um, the threshold voltage is 0.37 V, $Wg1$ and $Wg2$ are 300 um, $Wg3$ is 5 um, $Wg4$ is 15 um, $R1$ is 4.7 kΩ, $C1$ is 0.32 pF, and $C2$ is 0.061 pF.

[0054] FIG. 6 is a chart illustrating S parameter being input/output characteristics at Band41 in the case of the aforementioned circuit constants.

[0055] As illustrated in the chart, it is found that the curve of S21 takes a high value in a focused frequency range. On the other hand, curves of S11 and S22 take low values in the focused frequency range.

[0056] The gain at the center of the range is excellent such as 18.1 dB, and both S11 and S22 in the range are -13 dB or lower and satisfy the general requirement. In this embodiment, a bias current Idd_Ina is 6.12 mA which is large by the bias current (153 uA) in the IIP3 compensation circuit 10 as compared with the comparative example. The S parameter and NF according to this embodiment are substantially the same as the S parameter and NF in the comparative example.

[0057] FIG. 7 is a chart illustrating Pin dependence of the IIP3 according to this embodiment. The IIP3 when the power level of the input signal is -30 dBm is 15.8 dBm which is improved by 16.0 dB as compared with the comparative example.

[0058] As explained above, according to this embodiment, provision of the distortion compensation circuit enables realization of the LNA excellent in IIP3. The distortion compensation circuit according to this embodiment can be mounted on an SOI, and therefore can achieve downsizing and reduction in power consumption.

Third Embodiment

[0059] FIG. 8 is a diagram illustrating an LNA1 according to a third embodiment. In the LNA1 according to this embodiment, an IIP3 compensation circuit 10 includes a third transistor FET3, a fourth transistor FET4, and a first resistor R1 which are connected in series between a power supply node VDD_LNA being an output of an internal voltage regulator and the ground point, and further includes a first capacitor C1.

[0060] The third transistor FET3 has a drain and a gate connected to each other, and the drain and the gate are connected to the power supply node VDD_LNA. The fourth transistor FET4 has a drain and a gate connected to each other, and the drain and the gate are connected to a source of the third transistor FET3. The first resistor R1 has one terminal connected to a source of the fourth transistor FET4, and has another terminal which is grounded. In other words, the fourth transistor FET4 has the source which is grounded via the first resistor R1.

[0061] The capacitor C1 connects the first node n1 and the second node n2.

[0062] In this embodiment, the gate widths of the third transistor FET3 and the fourth transistor FET4 satisfy $Wg4 < Wg3$.

[0063] For example, regarding each transistor, the gate oxide film thickness is 2.5 nm, the gate length is 0.14 μ m, the threshold voltage is 0.37 V, Wg1 and Wg2 are 300 μ m, Wg3 is 15 μ m, Wg4 is 5 μ m, R1 is 6.2 k Ω , C1 is 0.34 pF.

[0064] FIG. 9 is a chart illustrating S parameter being input/output characteristics at Band41 in the case of the aforementioned circuit constants.

[0065] As illustrated in the chart, it is found that the curve of S21 takes a high value in a focused frequency range. On the other hand, curves of S11 and S22 take low values in the focused frequency range.

[0066] The gain at the center of the range is excellent such as 18.2 dB, and both S11 and S22 in the range are -13 dB or lower and satisfy the general requirement. In this embodiment, a bias current Idd_Ina is 6.088 mA which is large by the bias current (121 μ A) in the IIP3 compensation circuit 10 as compared with the comparative example. The S parameter and NF according to this embodiment are substantially the same as the S parameter and NF in the comparative example.

[0067] FIG. 10 is a chart illustrating Pin dependence of the IIP3 according to this embodiment. The IIP3 when the power level of the input signal is -30 dBm is 11.3 dBm which is improved by 11.5 dB as compared with the comparative example.

[0068] As explained above, according to this embodiment, provision of the distortion compensation circuit enables realization of the LNA excellent in IIP3. The distortion compensation circuit according to this embodiment can be mounted on an SOI, and therefore can achieve downsizing and reduction in power consumption.

[0069] Note that even when the connection order of the fourth transistor FET4 and the first resistor R1 is reversed, the same characteristics can be obtained in this embodiment.

Forth Embodiment

[0070] FIG. 11 is a diagram illustrating an LNA1 according to a forth embodiment. In the LNA1 according to this embodiment, an IIP3 compensation circuit 10 includes a first resistor R1, a third transistor FET3, and a fourth transistor FET4 which are connected in series between a power supply node VDD_LNA being an output of an internal voltage regulator and the ground point, and further includes a first capacitor C1.

[0071] The first resistor R1 has one terminal connected to the power supply node VDD_LNA. The third transistor FET3 has a drain and a gate connected to each other, and the drain and the gate are connected to another terminal of the first resistor R1. In other words, the third transistor FET3 has

the drain and the gate connected to the power supply node VDD_LNA via the first resistor R1. The fourth transistor FET4 has a drain and a gate connected to each other, and the drain and the gate are connected to a source of the third transistor FET3, and the fourth transistor FET4 has a source which is grounded.

[0072] The capacitor C1 connects the first node n1 and the second node n2.

[0073] In this embodiment, the gate widths of the third transistor FET3 and the fourth transistor FET4 satisfy $Wg3 < Wg4$.

[0074] For example, regarding each transistor, the gate oxide film thickness is 2.5 nm, the gate length is 0.14 μ m, the threshold voltage is 0.37 V, Wg1 and Wg2 are 300 μ m, Wg3 is 5 μ m, Wg4 is 20 μ m, R1 is 6.0 k Ω , C1 is 0.32 pF.

[0075] FIG. 12 is a chart illustrating S parameter being input/output characteristics at Band41 in the case of the aforementioned circuit constants.

[0076] As illustrated in the chart, it is found that the curve of S21 takes a high value in a focused frequency range. On the other hand, curves of S11 and S22 take low values in the focused frequency range.

[0077] The gain at the center of the range is excellent such as 18.2 dB, and both S11 and S22 in the range are -13 dB or lower and satisfy the general requirement. In this embodiment, a bias current Idd_Ina is 6.094 mA which is large by the bias current (127 μ A) in the IIP3 compensation circuit 10 as compared with the comparative example. The S parameter and NF according to this embodiment are substantially the same as the S parameter and NF in the comparative example.

[0078] FIG. 13 is a chart illustrating Pin dependence of the IIP3 according to this embodiment. The IIP3 when the power level of the input signal is -30 dBm is 11.9 dBm which is improved by 12.1 dB as compared with the comparative example.

[0079] As explained above, according to this embodiment, provision of the distortion compensation circuit enables realization of the LNA excellent in IIP3. The distortion compensation circuit according to this embodiment can be mounted on an SOI, and therefore can achieve downsizing and reduction in power consumption.

[0080] Note that even when the connection order of the third transistor FET3 and the first resistor R1 is reversed, the same characteristics can be obtained in this embodiment.

Fifth Embodiment

[0081] FIG. 14 is a diagram illustrating an LNA1 according to a fifth embodiment. In the LNA1 according to this embodiment, an IIP3 compensation circuit 10 includes a first resistor R1, a fifth transistor FET5, a third transistor FET3, and a fourth transistor FET4 which are connected in series between a power supply node VDD_LNA being an output of an internal voltage regulator and the ground point, and further includes a first capacitor C1, a second capacitor C2, and a third capacitor C3.

[0082] The first resistor R1 has one terminal connected to the power supply node VDD_LNA. The fifth transistor FET5 has a drain and a gate connected to each other, and the drain and the gate are connected to another terminal of the first resistor R1. In other words, the fifth transistor FET5 has the drain and the gate connected to the power supply node VDD_LNA via the first resistor R1. The third transistor FET3 has a drain and a gate connected to each other, and the

drain and the gate are connected to a source of the fifth transistor FET5. The fourth transistor FET4 has a drain and a gate connected to each other, and the drain and the gate are connected to a source of the third transistor FET3, and the fourth transistor FET4 has a source which is grounded.

[0083] The capacitor C1 connects the first node n1 and the second node n2. The second capacitor C2 connects the first node n1 and a fifth node n5 between the drain of the third transistor FET3 and the source of the fifth transistor FET5. The third capacitor C3 connects the first node n1 and a sixth node n6 between the first resistor R1 and the drain of the fifth transistor FET5.

[0084] In this embodiment, the gate widths of the third transistor FET3, the fourth transistor FET4, and the fifth transistor FET5 satisfy $Wg5 < Wg3 < Wg4$, and the electrostatic capacitances thereof satisfy $C2 < C1$ and $C3 < C1$.

[0085] For example, regarding each transistor, the gate oxide film thickness is 2.5 nm, the gate length is 0.14 μm , the threshold voltage is 0.37 V, $Wg1$ and $Wg2$ are 300 μm , $Wg3$ is 10 μm , $Wg4$ is 15 μm , $Wg5$ is 5 μm , $R1$ is 1.21 k Ω , $C1$ is 0.462 pF, $C2$ is 26.8 fF, and $C3$ is 42.1 fF.

[0086] FIG. 15 is a chart illustrating S parameter being input/output characteristics at Band41 in the case of the aforementioned circuit constants.

[0087] As illustrated in the chart, it is found that the curve of S21 takes a high value in a focused frequency range. On the other hand, curves of S11 and S22 take low values in the focused frequency range.

[0088] The gain at the center of the range is excellent such as 18.0 dB, and both S11 and S22 in the range are -13 dB or lower and satisfy the general requirement. In this embodiment, a bias current I_{dd_Ina} is 6.12 mA which is large by the bias current (155 μA) in the IIP3 compensation circuit 10 as compared with the comparative example. The S parameter and NF according to this embodiment are substantially the same as the S parameter and NF in the comparative example.

[0089] FIG. 16 is a chart illustrating Pin dependence of the IIP3 according to this embodiment. The IIP3 when the power level of the input signal is -30 dBm is 16.3 dBm which is improved by 16.5 dB as compared with the comparative example.

[0090] As explained above, according to this embodiment, provision of the distortion compensation circuit enables realization of the LNA excellent in IIP3. The distortion compensation circuit according to this embodiment can be mounted on an SOI, and therefore can achieve downsizing and reduction in power consumption.

Sixth Embodiment

[0091] FIG. 17 is a diagram illustrating an LNA1 according to a sixth embodiment. In the LNA1 according to this embodiment, an IIP3 compensation circuit 10 includes a third transistor FET3, and a fourth transistor FET4, and a fifth transistor FET5, and a first resistor R1 which are connected in series between a power supply node VDD_LNA being an output of an internal voltage regulator and the ground point, and further includes a first capacitor C1, a second capacitor C2, and a third capacitor C3.

[0092] The third transistor FET3 has a drain and a gate connected to each other, and the drain and the gate are connected to the power supply node VDD_LNA. The fourth transistor FET4 has a drain and a gate connected to each other, and the drain and the gate are connected to a source of the third transistor FET3. The fifth transistor FET5 has a

drain and gate connected to each other, and the drain and the gate connected to a source of the fourth transistor FET4. The first capacitor R1 has one terminal connected to a source of the fifth transistor FET5, and another terminal which is grounded. In other words, the fifth transistor FET5 has the source which is grounded via the first transistor R1.

[0093] The capacitor C1 connects the first node n1 and the second node n2. The second capacitor C2 connects the first node n1 and a seventh node n7 between the source of the fourth transistor FET4 and the drain of the fifth transistor FET5. The third capacitor C3 connects the first node n1 and an eighth node n8 between the first resistor R1 and the source of the fifth transistor FET5.

[0094] In this embodiment, the gate widths of the third transistor FET3, the fourth transistor FET4, and the fifth transistor FET5 satisfy $Wg5 < Wg4 < Wg3$, and the electrostatic capacitances thereof satisfy $C2 < C1$ and $C3 < C1$.

[0095] For example, regarding each transistor, the gate oxide film thickness is 2.5 nm, the gate length is 0.14 μm , the threshold voltage is 0.37 V, $Wg1$ and $Wg2$ are 300 μm , $Wg3$ is 15 μm , $Wg4$ is 10 μm , $Wg5$ is 5 μm , $R1$ is 1.22 k Ω , $C1$ is 0.394 pF, $C2$ is 34.7 fF, and $C3$ is 45.7 fF.

[0096] FIG. 18 is a chart illustrating S parameter being input/output characteristics at Band41 in the case of the aforementioned circuit constants.

[0097] As illustrated in the chart, it is found that the curve of S21 takes a high value in a focused frequency range. On the other hand, curves of S11 and S22 take low values in the focused frequency range.

[0098] The gain at the center of the range is excellent such as 18.0 dB, and both S11 and S22 in the range are -13 dB or lower and satisfy the general requirement. In this embodiment, a bias current I_{dd_Ina} is 6.12 mA which is large by the bias current (155 μA) in the IIP3 compensation circuit 10 as compared with the comparative example. The S parameter and NF according to this embodiment are substantially the same as the S parameter and NF in the comparative example.

[0099] FIG. 19 is a chart illustrating Pin dependence of the IIP3 according to this embodiment. The IIP3 when the power level of the input signal is -30 dBm is 17.7 dBm which is improved by 17.9 dB as compared with the comparative example.

[0100] As explained above, according to this embodiment, provision of the distortion compensation circuit enables realization of the LNA excellent in IIP3. The distortion compensation circuit according to this embodiment can be mounted on an SOI, and therefore can achieve downsizing and reduction in power consumption.

[0101] As explained above, for the LNA1 according to the first embodiment to the sixth embodiment, as a common configuration of the IIP3 compensation circuit (distortion compensation circuit) 10, an excellent IIP3 is realized by making the gate width smaller in a transistor closer to a position where the first resistor R1 is connected. Similarly, when a plurality of capacitors exist, a capacitor to which the largest number of transistors are connected in series between the capacitor and the first resistor R1 has a larger electrostatic capacitance than those of other capacitors, on the opposite side to the first node.

Seventh Embodiment

[0102] FIG. 20 is a diagram illustrating an LNA1 according to a seventh embodiment. The IIP3 compensation circuit (distortion compensation circuit) 10 includes the transistors

connected in series in each of the above-explained embodiments, and further includes transistors in parallel with the aforementioned transistors in this embodiment.

[0103] More specifically, in the LNA1 according to this embodiment, the IIP3 compensation circuit (distortion compensation circuit) 10 includes a third transistor FET3, a fourth transistor FET4, a first resistor R1, a first capacitor C1, and a second capacitor C2 which are connected in series between a power supply node VDD_LNA an output of an internal voltage regulator and the ground point, and further includes, in parallel with the above circuit, a second resistor R2, a fifth transistor FET5, a sixth transistor FET6, a third capacitor C3, and a fourth capacitor C4 which are connected in series between the power supply node VDD_LNA and the ground point.

[0104] The connection of the third transistor FET3, the fourth transistor FET4, the first resistor R1, the first capacitor C1, and the second capacitor C2 is the same as that in the first embodiment.

[0105] The second resistor R2 has one terminal connected to the power supply node VDD_LNA. The fifth transistor FET5 has a drain and a gate connected to each other, and the drain and the gate connected to another terminal of the second resistor R2. In other words, the fifth transistor FET5 has the drain and the gate connected the power supply node VDD_LNA via the second resistor R2. The sixth transistor FET6 has a drain and a gate connected to each other, and the drain and the gate connected to a source of the fifth transistor FET5, and the sixth transistor FET6 has a source which is grounded.

[0106] The third capacitor C3 connects the first node n1 and a ninth node n9 between the source of the fifth transistor FET5 and the drain of the sixth transistor FET6. The fourth capacitor C4 connects the first node n1 and a tenth node n10 between the drain of the fifth transistor FET5 and the second resistor R2.

[0107] In this embodiment, the gate widths of the third transistor FET3, the fourth transistor FET4, the fifth transistor FET5, and the sixth transistor FET6 satisfy $Wg4 < Wg3$, $Wg3 = Wg6$, and $Wg4 = Wg5$, the electrostatic capacitances thereof satisfy $C2 < C1$, $C1 = C3$, and $C2 = C4$, and the resistor thereof satisfy $R1 = R2$.

[0108] For example, regarding each transistor, the gate oxide film thickness is 2.5 nm, the gate length is 0.14 μm , the threshold voltage is 0.37 V, $Wg1$ and $Wg2$ are 300 μm , $Wg3$ and $Wg6$ are 7.5 μm , $Wg4$ and $Wg5$ are 2.5 μm , $R1$ and $R2$ are 8.8 k Ω , $C1$ and $C3$ are 0.180 pF, and $C2$ and $C4$ are 0.030 pF.

[0109] FIG. 21 is a chart illustrating S parameter being input/output characteristics at Band41 in the case of the aforementioned circuit constants.

[0110] As illustrated in the chart, it is found that the curve of S21 takes a high value in a focused frequency range. On the other hand, curves of S11 and S22 take low values in the focused frequency range.

[0111] The gain at the center of the range is excellent such as 18.1 dB, and both S11 and S22 in the range are -13 dB or lower and satisfy the general requirement. In this embodiment, a bias current I_{dd_Ina} is 6.128 nA which is large by the bias current (161 μA) in the IIP3 compensation circuit 10 as compared with the comparative example. The S parameter and NF according to this embodiment are substantially the same as the S parameter and NF in the comparative example.

[0112] FIG. 22 is a chart illustrating Pin dependence of the IIP3 according to this embodiment. The IIP3 when the power level of the input signal is -30 dBm is 18.1 dBm which is improved by 18.3 dB as compared with the comparative example.

[0113] As explained above, according to this embodiment, provision of the distortion compensation circuit enables realization of the LNA excellent in IIP3. The distortion compensation circuit according to this embodiment can be mounted on an SOI, and therefore can achieve downsizing and reduction in power consumption.

[0114] Note that the transistors for signal amplification in the amplifier circuit are configured at two stages in all of the above-explained embodiments, but may be configured at three stages. For example, the LNA1 may include a transistor having a gate grounded similarly in a high-frequency manner between the second transistor and the output port LNAout (and the output matching circuit) in addition to the first transistor FET1 and the second transistor FET2. In this case, the IIP3 compensation circuit 10 is desirably connected not to the source but to the drain of the FET2.

[0115] In each of the above-explained embodiments, having the same circuit constant means that the circuit constant does have to be strictly the same and, for example, only needs to be the same in a range where an individual difference or the like may arise even in elements having the same circuit constant.

[0116] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

[0117] For example, in all of the above-explained embodiments, the n-type MOSFET may be a p-type MOSFET according to the situation and the p-type MOSFET may be an n-type MOSFET according to the situation. Further, as the MOSFET, another transistor having the same function, for example, the one which functions as a switching element by voltage, current, or another external switching signal, such as a bipolar transistor may be used. For example, in the case of using the bipolar transistor, the gate, source, drain in the explanation in this specification and claims may be replaced in reading with an appropriate combination of a base, a collector (emitter), and an emitter (collector), respectively. In any replacement in reading, the physical amount used for switching such as the magnitude of the voltage to be applied to the gate, the current to be applied to the base or the like can be appropriately replaced in reading so as to appropriately perform the equivalent operation as the one having the above-described functions by the characteristics of the elements.

1. A high-frequency amplifier circuitry, comprising:
 - an amplifier circuit, the amplifier circuit comprising:
 - a first transistor having a gate to which an input signal is applied;
 - an inductor having one terminal which is connected to a source of the first transistor and another terminal which is grounded; and

- a second transistor having a source which is connected to a drain of the first transistor, a gate which is grounded, and a drain which is connected to a power supply voltage terminal, the second transistor configured to output from the drain a signal obtained by amplifying the input signal; and
- a distortion compensation circuit, the distortion compensation circuit comprising:
- a third transistor having a drain and a gate which are connected to each other, the third transistor connected to the power supply voltage terminal on the drain side;
 - a fourth transistor having a drain and a gate which are connected to a source of the third transistor, the fourth transistor grounded on a source side; and
 - a first capacitor connecting a node between the drain of the first transistor and the source of the second transistor, and, the source of the third transistor.
2. The high-frequency amplifier circuitry according to claim 1, further comprising:
- an input matching circuit connecting to the gate of the first transistor and to an input terminal for the input signal; and
 - an output matching circuit connecting to the drain of the second transistor, to the power supply voltage terminal, and to an output terminal.
3. The high-frequency amplifier circuitry according to claim 1, wherein:
- the distortion compensation circuit further comprises a first resistor, the first resistor connecting the source of the fourth transistor and a ground point; and
 - a gate width of the fourth transistor is narrower than a gate width of the third transistor.
4. The high-frequency amplifier circuitry according to claim 3, wherein:
- the distortion compensation circuit further comprises a second capacitor, the second capacitor connecting the node and the source of the fourth transistor; and
 - an electrostatic capacitance of the second capacitor is smaller than an electrostatic capacitance of the first capacitor.
5. The high-frequency amplifier circuitry according to claim 4, wherein:
- the distortion compensation circuit further comprises:
 - a fifth transistor between the source of the fourth transistor and the first resistor, the fifth transistor having a drain and a gate which are connected to the source of the fourth transistor and a source which is connected to the first resistor; and
 - a third capacitor connecting the node and the source of the fifth transistor;
 - a gate width of the fifth transistor is narrower than the gate width of the fourth transistor; and
 - an electrostatic capacitance of the third capacitor is smaller than the electrostatic capacitance of the first capacitor.
6. The high-frequency amplifier circuitry according to claim 4, wherein
- the distortion compensation circuit further comprises:
 - a second resistor having a same resistance value as a resistance value of the first resistor, the second resistor connecting to the power supply voltage terminal;
 - a fifth transistor having a same gate width as the gate width of the fourth transistor, and having a drain and a gate which are connected to the power supply voltage terminal via the second resistor;
 - a sixth transistor having a same gate width as the gate width of the third transistor, and having a drain and a gate which are connected to the source of the fifth transistor and a source which is grounded;
 - a third capacitor having a same electrostatic capacitance as the electrostatic capacitance of the first capacitor, the third capacitor connecting the node and the source of the fifth transistor; and
 - a fourth capacitor having a same electrostatic capacitance as the electrostatic capacitance of the second capacitor, the fourth capacitor connecting the node and the drain of the fifth transistor.
7. The high-frequency amplifier circuitry according to claim 1, wherein
- the distortion compensation circuit further comprises a first resistor, the first resistor connecting the drain of the third transistor and the power supply voltage terminal; and
 - a gate width of the third transistor is narrower than a gate width of the fourth transistor.
8. The high-frequency amplifier circuitry according to claim 7, wherein:
- the distortion compensation circuit further comprises a second capacitor, the second capacitor connecting the node and the drain of the third transistor; and
 - an electrostatic capacitance of the second capacitor is smaller than an electrostatic capacitance of the first capacitor.
9. The high-frequency amplifier circuitry according to claim 8, wherein:
- the distortion compensation circuit further comprises:
 - a fifth transistor between the drain of the third transistor and the first resistor, the fifth transistor having a drain and a gate which are connected to the first resistor and a source which is connected to the drain of the third transistor; and
 - a third capacitor connecting the node and the drain of the fifth transistor;
 - a gate width of the fifth transistor is narrower than the gate width of the third transistor; and
 - an electrostatic capacitance of the third capacitor is smaller than the electrostatic capacitance of the first capacitor.
10. The high-frequency amplifier circuitry according to claim 2, wherein
- the distortion compensation circuit further comprises a first resistor, the first resistor connecting the source of the fourth transistor and a ground point; and
 - a gate width of the fourth transistor is narrower than a gate width of the third transistor.
11. The high-frequency amplifier circuitry according to claim 10 wherein
- the distortion compensation circuit further comprises a second capacitor, the second capacitor connecting the node and the source of the fourth transistor; and
 - an electrostatic capacitance of the second capacitor is smaller than an electrostatic capacitance of the first capacitor.
12. The high-frequency amplifier circuitry according to claim 11, wherein:

the distortion compensation circuit further comprises:
 a fifth transistor between the source of the fourth transistor and the first resistor, the fifth transistor having a drain and a gate which are connected to the source of the fourth transistor and a source which is connected to the first resistor; and
 a third capacitor connecting the node and the source of the fifth transistor;
 a gate width of the fifth transistor is narrower than the gate width of the fourth transistor; and
 an electrostatic capacitance of the third capacitor is smaller than the electrostatic capacitance of the first capacitor.

13. The high-frequency amplifier circuitry according to claim **11**, wherein

the distortion compensation circuit further comprises:
 a second resistor having a same resistance value as a resistance value of the first resistor, the second resistor connecting to the power supply voltage terminal;
 a fifth transistor having a same gate width as the gate width of the fourth transistor, and having a drain and a gate which are connected to the power supply voltage terminal via the second resistor;
 a sixth transistor having a same gate width as the gate width of the third transistor, and having a drain and a gate which are connected to the source of the fifth transistor and a source which is grounded;
 a third capacitor having a same electrostatic capacitance as the electrostatic capacitance of the first capacitor, the third capacitor connecting the node and the source of the fifth transistor; and
 a fourth capacitor having a same electrostatic capacitance as the electrostatic capacitance of the second capacitor, the fourth capacitor connecting the node and the drain of the fifth transistor.

14. The high-frequency amplifier circuitry according to claim **2**, wherein:

the distortion compensation circuit further comprises a first resistor, the first resistor connecting the drain of the third transistor and the power supply voltage terminal; and
 a gate width of the third transistor is narrower than a gate width of the fourth transistor.

15. The high-frequency amplifier circuitry according to claim **14**, wherein:

the distortion compensation circuit further comprises a second capacitor, the second capacitor connecting the node and the source of the third transistor; and
 an electrostatic capacitance of the second capacitor is smaller than an electrostatic capacitance of the first capacitor.

16. The high-frequency amplifier circuitry according to claim **15**, wherein

the distortion compensation circuit further comprises:
 a fifth transistor between the drain of the third transistor and the first resistor, the fifth transistor having a drain and a gate which are connected to the first resistor and a source which is connected to the drain of the third transistor; and
 a third capacitor connecting the node and the drain of the fifth transistor;
 a gate width of the fifth transistor is narrower than the gate width of the third transistor; and
 an electrostatic capacitance of the third capacitor is smaller than the electrostatic capacitance of the first capacitor.

17. A semiconductor device comprising at least one high-frequency amplifier circuitry on a silicon on insulator (SOI) substrate,

the at least one high-frequency amplifier circuitry comprising:

an amplifier circuit, the amplifier circuit comprising:
 a first transistor having a gate to which an input signal is applied;
 an inductor having one terminal which is connected to a source of the first transistor and another terminal which is grounded; and
 a second transistor having a source which is connected to a drain of the first transistor, a gate which is grounded, and a drain which is connected to a power supply voltage terminal, the second transistor configured to output from the drain a signal obtained by amplifying the input signal; and

a distortion compensation circuit, the distortion compensation circuit comprising:

a third transistor having a drain and a gate which are connected to each other, the third transistor connected to the power supply voltage terminal on the drain side;
 a fourth transistor having a drain and a gate which are connected to a source of the third transistor, the fourth transistor grounded on a source side; and
 a first capacitor connecting a node between the drain of the first transistor and the source of the second transistor, and, the source of the third transistor.

18. The semiconductor device according to claim **17**, wherein the at least one high-frequency amplifier circuitry further comprises:

an input matching circuit connecting to the gate of the first transistor and to an input terminal for the input signal; and
 an output matching circuit connecting to the drain of the second transistor, to the power supply voltage terminal, and to an output terminal.

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