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(54) **HIGH SPEED SIGNAL DRIVE CIRCUIT**

(71) Applicant: **LONTIUM SEMICONDUCTOR CORPORATION**, Hefei (CN)

(72) Inventors: **Xiangyu JI**, Hefei (CN); **Cheng TAO**, Hefei (CN); **Yu CHEN**, Hefei (CN); **Feng CHEN**, Hefei (CN); **Jiaxi FU**, Hefei (CN); **Haiyan WEI**, Hefei (CN)

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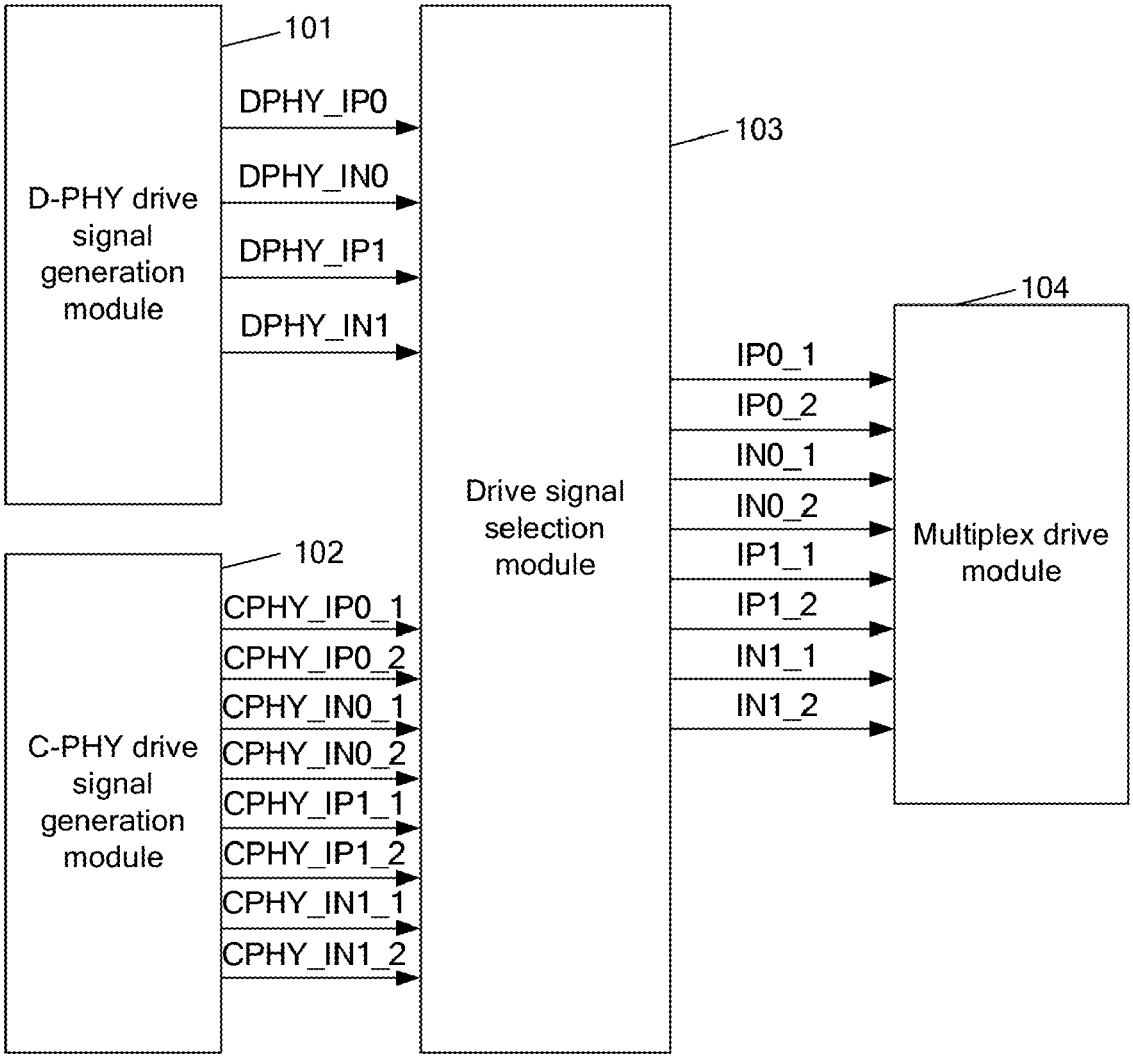
(57) **ABSTRACT**

A high speed signal drive circuit includes a D-PHY drive signal generation module, a C-PHY drive signal generation module, a drive signal selection module and a multiplex drive module. An output terminal of the D-PHY drive signal generation module and an output terminal of the C-PHY drive signal generation module are both connected to an input terminal of the drive signal selection module. An output terminal of the drive signal selection module is connected to an input terminal of the multiplex drive module. The drive signal selection module controls control switches of the multiplex drive module to be on and off based on a D-PHY drive signal or a C-PHY drive signal, so that the multiplex drive module functions as a D-PHY drive circuit or a C-PHY drive circuit. Thus, dual functions of the D-PHY drive circuit and the C-PHY drive circuit can be realized.



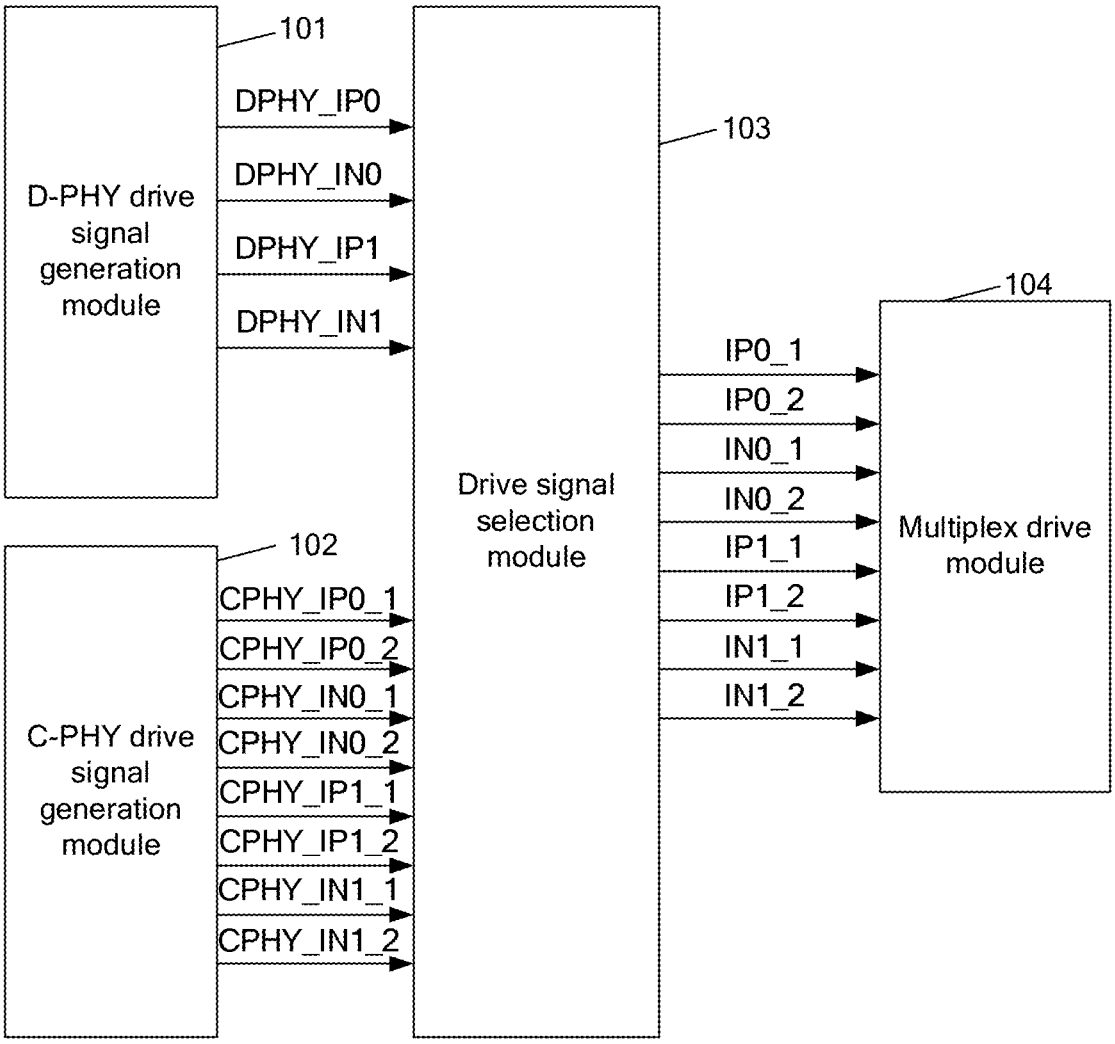

101
D-PHY drive signal generation module
DPHY_IP0
DPHY_IN0
DPHY_IP1
DPHY_IN1
102
C-PHY drive signal generation module
CPHY_IP0_1
CPHY_IP0_2
CPHY_IN0_1
CPHY_IN0_2
CPHY_IP1_1
CPHY_IP1_2
CPHY_IN1_1
CPHY_IN1_2
Drive signal selection module
103
IP0_1
IP0_2
IN0_1
IN0_2
IP1_1
IP1_2
IN1_1
IN1_2
104
Multiplex drive module

FIG. 1

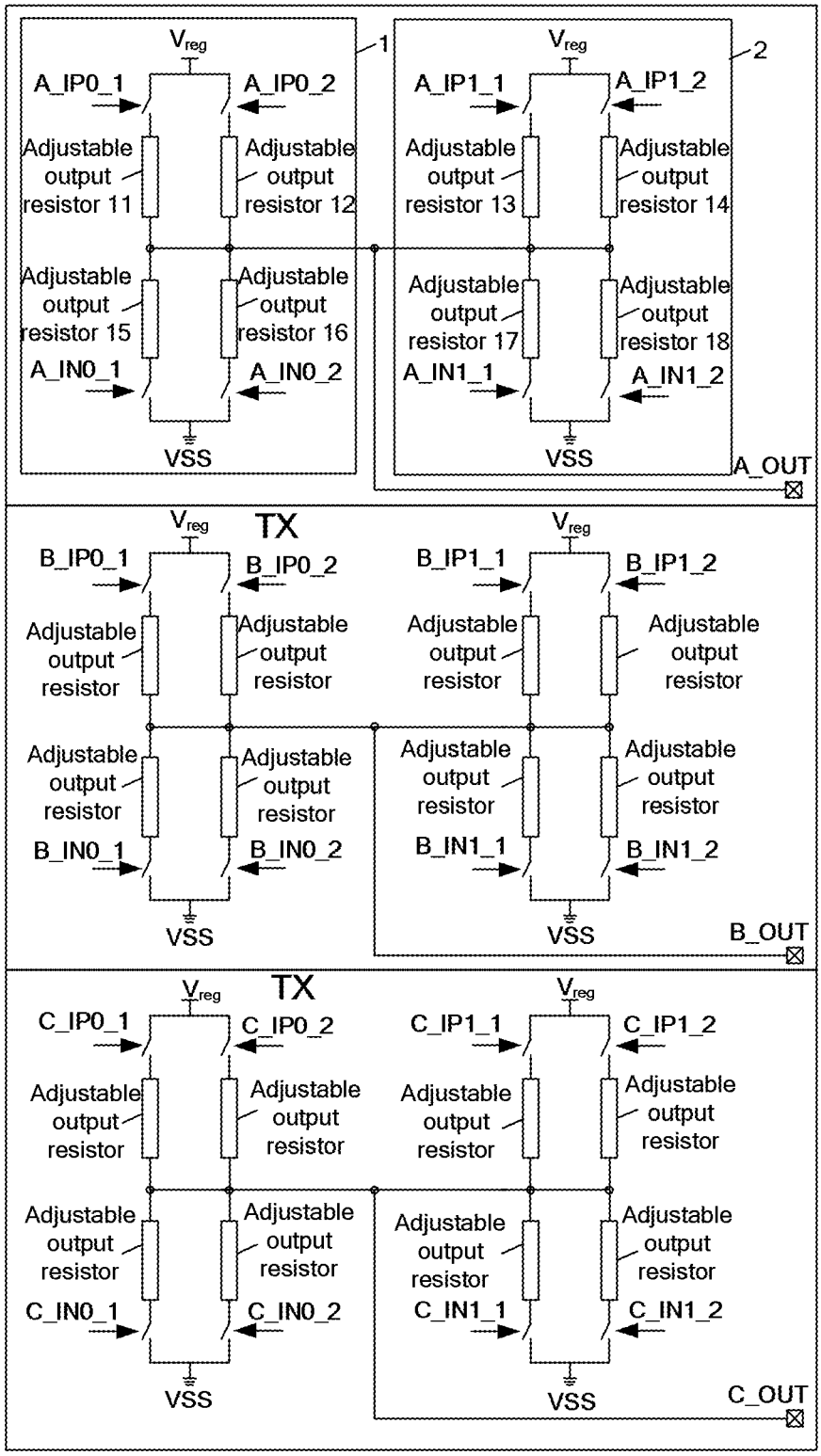

Vreg
1
A_IP0_1
A_IP0_2
Adjustable output resistor 11
Adjustable output resistor 12
Adjustable output resistor 15
Adjustable output resistor 16
A_IN0_1
A_IN0_2
VSS
Vreg
2
A_IP1_1
A_IP1_2
Adjustable output resistor 13
Adjustable output resistor 14
Adjustable output resistor 17
Adjustable output resistor 18
A_IN1_1
A_IN1_2
VSS
A_OUT
Vreg
TX
B_IP0_1
B_IP0_2
Adjustable output resistor
Adjustable output resistor
Adjustable output resistor
Adjustable output resistor
B_IN0_1
B_IN0_2
VSS
Vreg
B_IP1_1
B_IP1_2
Adjustable output resistor
Adjustable output resistor
Adjustable output resistor
Adjustable output resistor
B_IN1_1
B_IN1_2
VSS
B_OUT
Vreg
TX
C_IP0_1
C_IP0_2
Adjustable output resistor
Adjustable output resistor
Adjustable output resistor
Adjustable output resistor
C_IN0_1
C_IN0_2
VSS
Vreg
C_IP1_1
C_IP1_2
Adjustable output resistor
Adjustable output resistor
Adjustable output resistor
Adjustable output resistor
C_IN1_1
C_IN1_2
VSS
C_OUT

FIG. 2

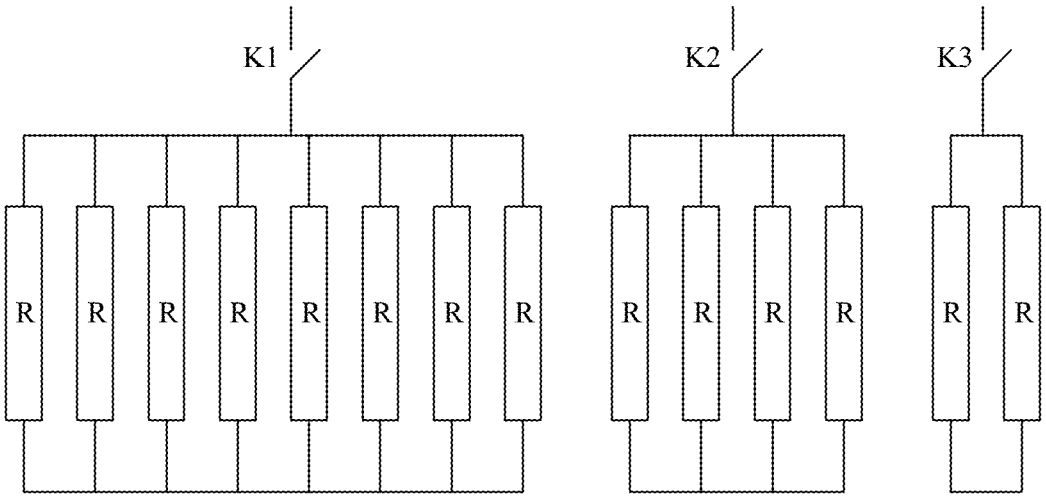


FIG. 3

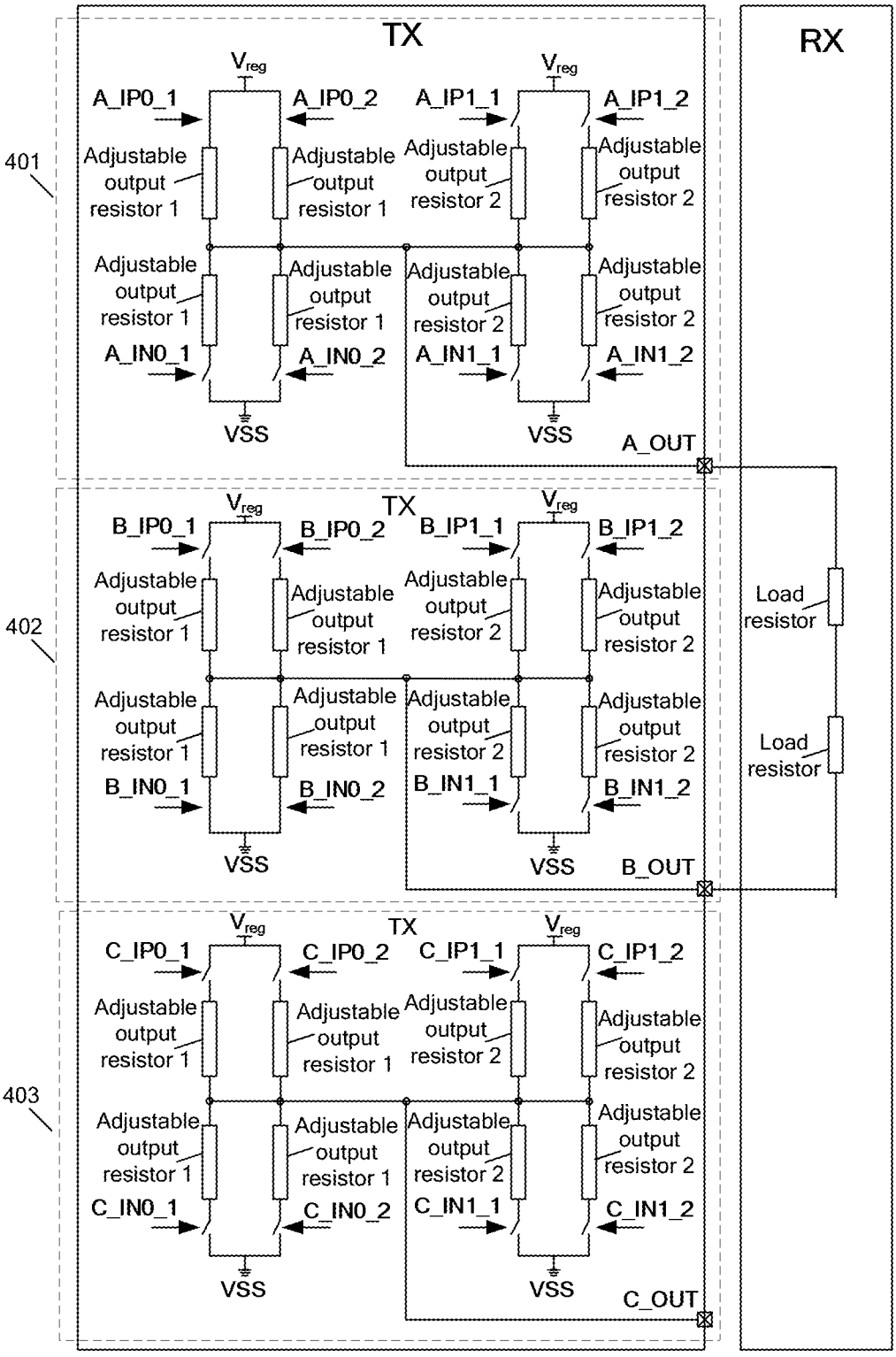

TX
RX
401
402
403
V_{reg}
A_IP0_1
A_IP0_2
A_IP1_1
A_IP1_2
Adjustable output resistor 1
Adjustable output resistor 2
A_IN0_1
A_IN0_2
A_IN1_1
A_IN1_2
VSS
A_OUT
B_IP0_1
B_IP0_2
B_IP1_1
B_IP1_2
B_IN0_1
B_IN0_2
B_IN1_1
B_IN1_2
B_OUT
Load resistor
C_IP0_1
C_IP0_2
C_IP1_1
C_IP1_2
C_IN0_1
C_IN0_2
C_IN1_1
C_IN1_2
C_OUT

FIG. 4

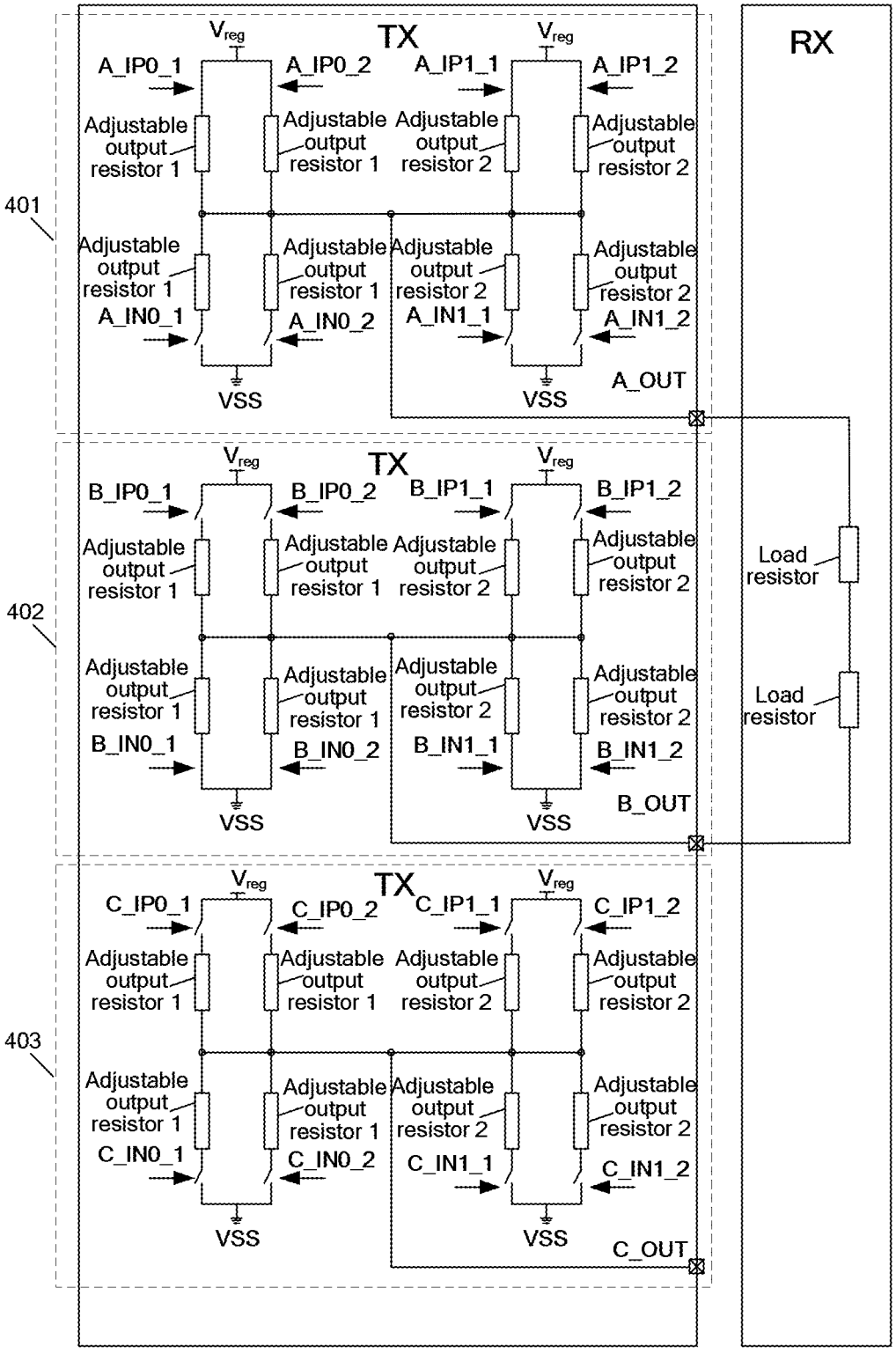

TX
RX
401
402
403
V_{reg}
A_IP0_1
A_IP0_2
A_IP1_1
A_IP1_2
Adjustable output resistor 1
Adjustable output resistor 2
A_IN0_1
A_IN0_2
A_IN1_1
A_IN1_2
VSS
A_OUT
B_IP0_1
B_IP0_2
B_IP1_1
B_IP1_2
B_IN0_1
B_IN0_2
B_IN1_1
B_IN1_2
B_OUT
C_IP0_1
C_IP0_2
C_IP1_1
C_IP1_2
C_IN0_1
C_IN0_2
C_IN1_1
C_IN1_2
C_OUT
Load resistor

FIG. 5

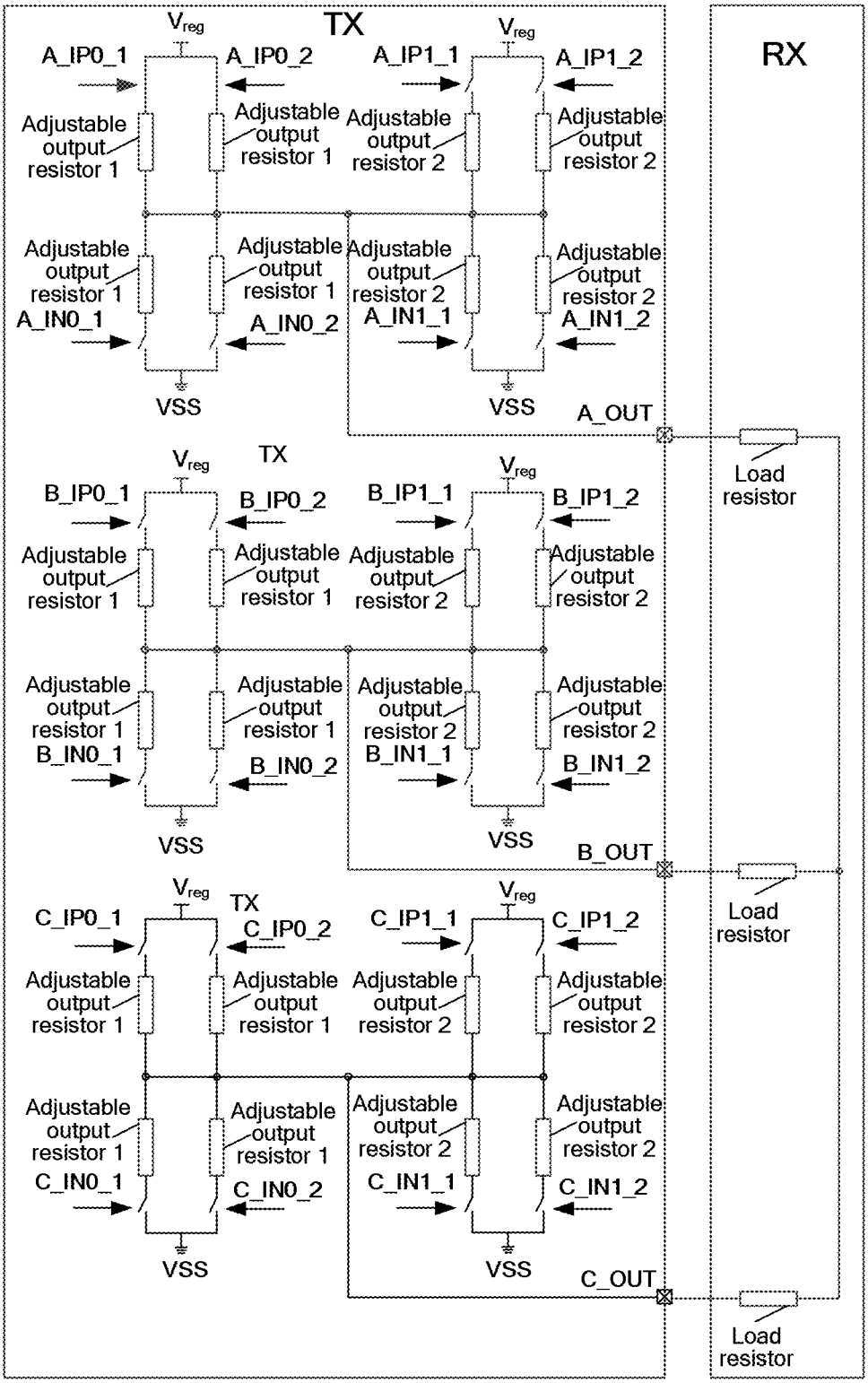

TX
RX
V_{reg}
A_IP0_1
A_IP0_2
A_IP1_1
A_IP1_2
Adjustable output resistor 1
Adjustable output resistor 2
A_IN0_1
A_IN0_2
A_IN1_1
A_IN1_2
VSS
A_OUT
Load resistor
B_IP0_1
B_IP0_2
B_IP1_1
B_IP1_2
B_IN0_1
B_IN0_2
B_IN1_1
B_IN1_2
B_OUT
C_IP0_1
C_IP0_2
C_IP1_1
C_IP1_2
C_IN0_1
C_IN0_2
C_IN1_1
C_IN1_2
C_OUT

FIG. 6

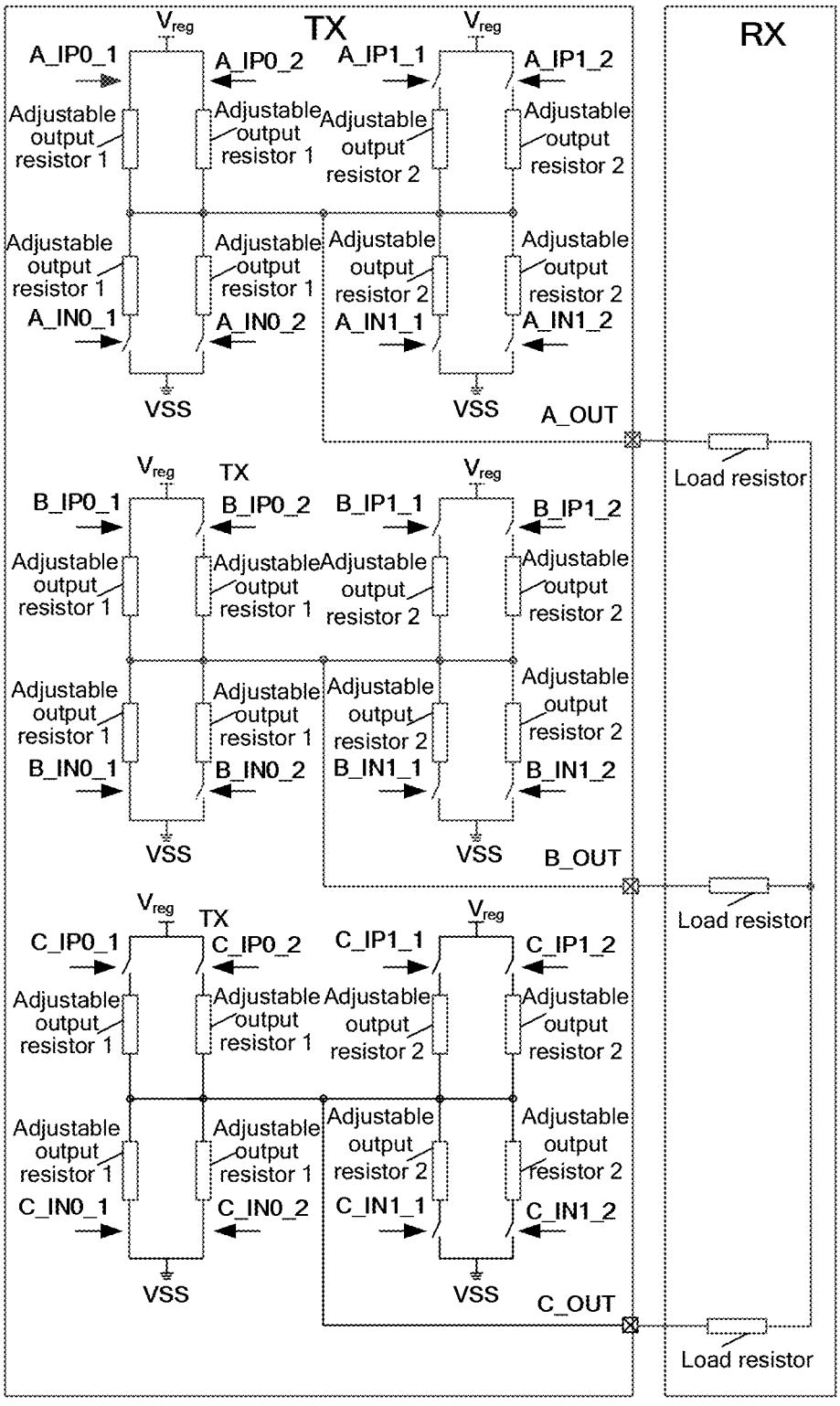

TX
RX
V_{reg}
A_IP0_1
A_IP0_2
A_IP1_1
A_IP1_2
Adjustable output resistor 1
Adjustable output resistor 2
A_IN0_1
A_IN0_2
A_IN1_1
A_IN1_2
VSS
A_OUT
Load resistor
B_IP0_1
B_IP0_2
B_IP1_1
B_IP1_2
B_IN0_1
B_IN0_2
B_IN1_1
B_IN1_2
B_OUT
C_IP0_1
C_IP0_2
C_IP1_1
C_IP1_2
C_IN0_1
C_IN0_2
C_IN1_1
C_IN1_2
C_OUT

FIG. 7

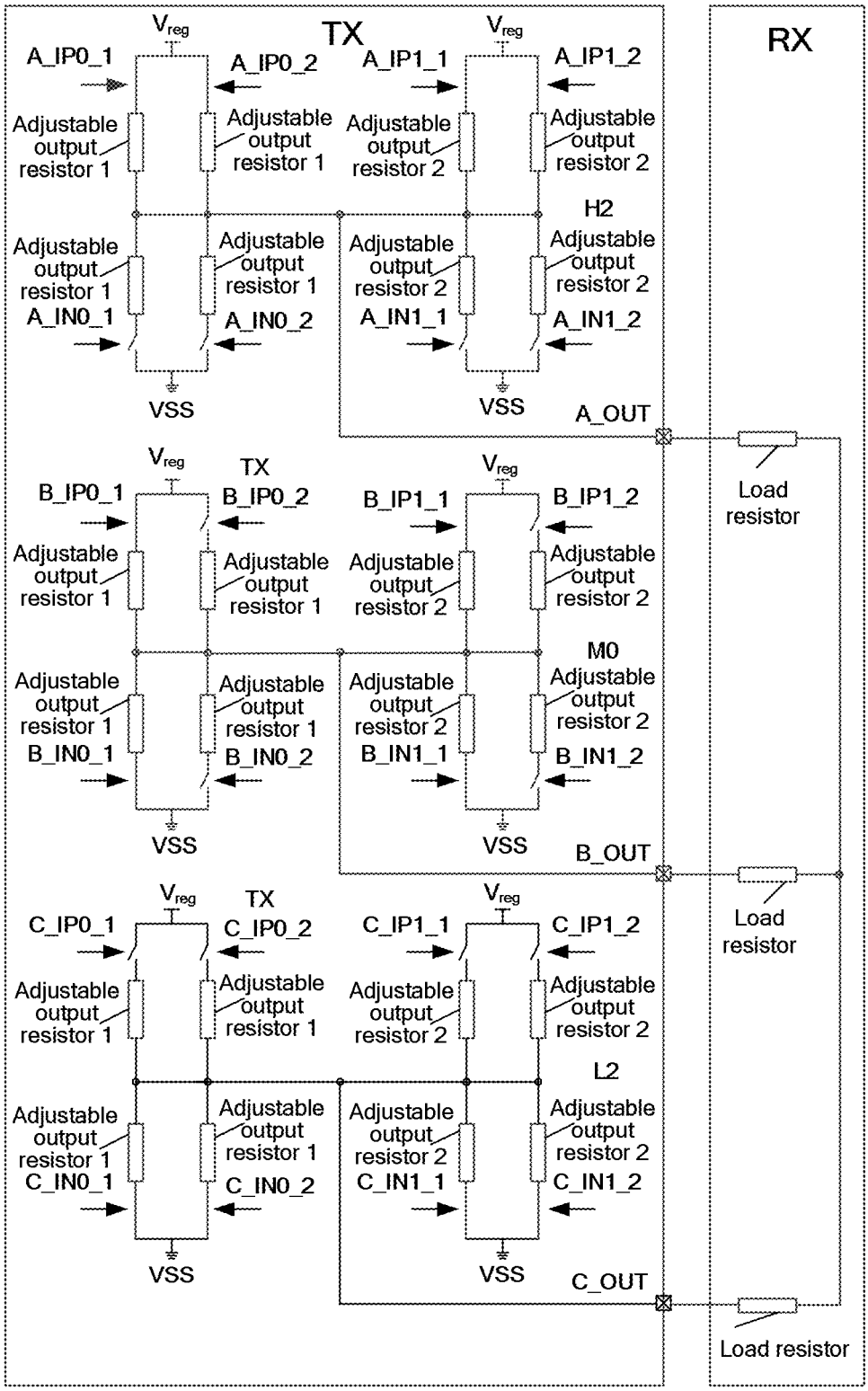

TX
RX
Vreg
A_IP0_1
A_IP0_2
A_IP1_1
A_IP1_2
Adjustable output resistor 1
Adjustable output resistor 2
H2
A_IN0_1
A_IN0_2
A_IN1_1
A_IN1_2
VSS
A_OUT
Load resistor
B_IP0_1
B_IP0_2
B_IP1_1
B_IP1_2
M0
B_IN0_1
B_IN0_2
B_IN1_1
B_IN1_2
B_OUT
C_IP0_1
C_IP0_2
C_IP1_1
C_IP1_2
L2
C_IN0_1
C_IN0_2
C_IN1_1
C_IN1_2
C_OUT

FIG. 8

HIGH SPEED SIGNAL DRIVE CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present invention claims priority under 35 U.S.C. § 119 to Chinese patent application No. 201910079310.X, filed Jan. 28, 2019, the entire contents of which are incorporated herein by reference.

FIELD

[0002] The present disclosure relates to the field of drive circuit, in particular to a high speed signal drive circuit.

BACKGROUND

[0003] D-PHY (Physical layer) and C-PHY (Physical layer) are physical layer interface standards of MIPI (Mobile Industry Processor Interface). Drive circuits corresponding to a D-PHY interface and a C-PHY interface are required when using the D-PHY interface and the C-PHY interface.

[0004] In the conventional technology, a D-PHY high speed drive circuit and a C-PHY high speed drive circuit are two independent circuits. A multiplex circuit combining the D-PHY high speed drive circuit with the C-PHY high speed drive circuit is cost-saving, and is a development trend of the MIPI. Therefore, it is desired to provide a high speed drive circuit having dual functions of the D-PHY high speed drive circuit and the C-PHY high speed drive circuit.

SUMMARY

[0005] In view of the above, the present disclosure provides a high speed signal drive circuit, which has dual functions of the D-PHY high speed drive circuit and the C-PHY high speed drive circuit.

[0006] To achieve the objective, the following technical solutions are provided according to the present disclosure.

[0007] A high speed signal drive circuit includes a D-PHY drive signal generation module, a C-PHY drive signal generation module, a drive signal selection module and a multiplex drive module,

[0008] where an output terminal of the D-PHY drive signal generation module and an output terminal of the C-PHY drive signal generation module are both connected to an input terminal of the drive signal selection module, and an output terminal of the drive signal selection module is connected to an input terminal of the multiplex drive module;

[0009] the D-PHY drive signal generation module is configured to generate a D-PHY drive signal;

[0010] the C-PHY drive signal generation module is configured to generate a C-PHY drive signal; and

[0011] the drive signal selection module is configured to: receive the D-PHY drive signal or the C-PHY drive signal, and control a control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, by which the multiplex drive module functions as a D-PHY drive circuit or a C-PHY drive circuit.

[0012] Preferably, the multiplex drive module includes at least three drive sub-modules, where each drive sub-module includes eight control switches and eight adjustable output resistors, each of four adjustable output resistors of the eight adjustable output resistors is connected to a termination power supply through a respective one of the eight control switches, each of another four adjustable output resistors of the eight adjustable output resistors is connected to a grounding terminal through a respective one of the eight control switches, and terminals of all the adjustable output resistors, which are not connected to the control switches, are connected to each other to function as an output terminal.

[0013] Preferably, in a case that the multiplex drive module is configured to function as the D-PHY drive circuit, output terminals of two drive sub-modules of the at least three drive sub-modules of the multiplex drive module are connected to each other through a load resistor.

[0014] Preferably, in a case that the multiplex drive module is configured to function as the C-PHY drive circuit, output terminals of three drive sub-modules of the at least three drive sub-modules of the multiplex drive circuit are connected to each other in a star connection through a load resistor.

[0015] Preferably, in receiving the D-PHY drive signal or the C-PHY drive signal and controlling the control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, by which the multiplex drive module functions as the D-PHY drive circuit or the C-PHY drive circuit, the drive signal selection module is configured to:

[0016] control, in a case that the D-PHY drive signal is a first primary drive control signal and the C-PHY drive signal is null, a control switch of the multiplex drive module corresponding to the first primary drive control signal to be closed, by which the multiplex drive module functions as the D-PHY drive circuit, where the first primary drive control signal includes a control signal of a D-PHY primary drive circuit and/or a control signal of a D-PHY pre-emphasis drive circuit.

[0017] Preferably, in receiving the D-PHY drive signal or the C-PHY drive signal and controlling the control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, by which the multiplex drive module functions as the D-PHY drive circuit or the C-PHY drive circuit, the drive signal selection module is configured to:

[0018] control, in a case that the C-PHY drive signal is a second primary drive control signal and the D-PHY drive signal is null, a control switch of the multiplex drive module corresponding to the second primary drive control signal to be closed, by which the multiplex drive module functions as the C-PHY drive circuit, where the second primary drive control signal includes a control signal of a C-PHY primary drive circuit and/or a control signal of a C-PHY pre-emphasis drive circuit.

[0019] Preferably, each two drive sub-modules of the at least three drive sub-modules function as an output channel of the D-PHY drive circuit, to realize multiple outputs of the D-PHY drive circuit.

[0020] Preferably, each three drive sub-modules of the at least three drive sub-modules function as an output channel of the C-PHY drive circuit, to realize multiple outputs of the C-PHY drive circuit.

[0021] Preferably, the adjustable output resistor includes multiple branches connected in parallel, and each of the multiple branches includes multiple resistor branches that are connected in parallel with each other and a switch connected in series with all the multiple resistor branches that are connected in parallel with each other.

[0022] Compared to the conventional technology, the present disclosure has the following beneficial effects.

[0023] A high speed signal drive circuit is provided according to the present disclosure. The high speed signal drive circuit includes a D-PHY drive signal generation module, a C-PHY drive signal generation module, a drive signal selection module and a multiplex drive module. An output terminal of the D-PHY drive signal generation module and an output terminal of the C-PHY drive signal generation module are both connected to an input terminal of the drive signal selection module. An output terminal of the drive signal selection module is connected to an input terminal of the multiplex drive module. The D-PHY drive signal generation module is configured to generate a D-PHY drive signal, and the C-PHY drive signal generation module is configured to generate a C-PHY drive signal. The drive signal selection module is configured to: receive the D-PHY drive signal or the C-PHY drive signal, and control a control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, so that the multiplex drive module realizes a function of a D-PHY drive circuit or a C-PHY drive circuit. In this way, dual functions of the D-PHY drive circuit and the C-PHY drive circuit can be realized merely by the high speed signal drive circuit according to the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] In order to more clearly illustrate technical solutions in embodiments of the present application or in the conventional technology, drawings used in the description of the embodiments or the conventional technology are introduced briefly hereinafter. Apparently, the drawings described in the following illustrate some embodiments of the present application, other drawings may be obtained by those ordinarily skilled in the art based on these drawings without any creative efforts.

[0025] FIG. **1** is a schematic structural diagram of a high speed signal drive circuit according to an embodiment of the present disclosure;

[0026] FIG. **2** is a schematic structural diagram of a multiplex drive module according to an embodiment of the present disclosure;

[0027] FIG. **3** is a schematic structural diagram of an adjustable output resistor according to an embodiment of the present disclosure;

[0028] FIG. **4** is a schematic structural diagram of a multiplex drive module according to an embodiment of the present disclosure;

[0029] FIG. **5** is a schematic structural diagram of a multiplex drive module according to an embodiment of the present disclosure;

[0030] FIG. **6** is a schematic structural diagram of a multiplex drive module according to an embodiment of the present disclosure;

[0031] FIG. **7** is a schematic structural diagram of a multiplex drive module according to an embodiment of the present disclosure; and

[0032] FIG. **8** is a schematic structural diagram of a multiplex drive module according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF EMBODIMENTS

[0033] The technical solutions in the embodiments of the present application will be described clearly and completely hereinafter in conjunction with the drawings in the embodiments of the present disclosure. Apparently, the described embodiments are only some rather than all of the embodiments of the present application. Based on the embodiments in the present disclosure, any other embodiments made by the person skilled in the art without any creative efforts fall within the scope of protection of the present disclosure.

[0034] A high speed signal drive circuit is provided according to an embodiment of the present disclosure.

[0035] Referring to FIG. **1**, the high speed signal drive circuit includes: a D-PHY drive signal generation module **101**, a C-PHY drive signal generation module **102**, a drive signal selection module **103** and a multiplex drive module **104**,

[0036] where an output terminal of the D-PHY drive signal generation module **101** and an output terminal of the C-PHY drive signal generation module **102** are both connected to an input terminal of the drive signal selection module **103**, and an output terminal of the drive signal selection module **103** is connected to an input terminal of the multiplex drive module **104**;

[0037] the D-PHY drive signal generation module **101** is configured to generate a D-PHY drive signal;

[0038] the C-PHY drive signal generation module **102** is configured to generate a C-PHY drive signal; and

[0039] the drive signal selection module **103** is configured to: receive the D-PHY drive signal or the C-PHY drive signal, and control a control switch of the multiplex drive module **104** to be on and off based on the D-PHY drive signal or the C-PHY drive signal, by which the multiplex drive module **104** functions as a D-PHY drive circuit or a C-PHY drive circuit.

[0040] In an embodiment, the D-PHY drive signal generation module **101** is configured to generate a control signal of a D-PHY primary drive circuit or a control signal of a D-PHY pre-emphasis circuit based on data to be sent by a D-PHY interface.

[0041] In an embodiment, the D-PHY drive signal generation module **101** is configured to generate control signals DPHY_IP**0** and DPHY_IN**0** of the D-PHY primary drive circuit, and control signals DPHY_IP**1** and DPHY_IN**1** of the D-PHY pre-emphasis circuit based on the data to be sent by the D-PHY interface.

[0042] The C-PHY drive signal generation module **102** is configured to convert an online state (including six states of +X, +Y, +Z, −X, −Y, and −Z, which are used as input signals) to be sent by a C-PHY interface into a control signal of a C-PHY primary drive circuit or a control signal of a C-PHY pre-emphasis drive circuit.

[0043] In an embodiment, the C-PHY drive signal generation module **102** is configured to convert an online state (including six states of +X, +Y, +Z, −X, −Y, and −Z, which are used as input signals) to be sent by the C-PHY interface into control signals CPHY_IP**0_1**, CPHY_IP**0_2**, CPHY_IN**0_1** and CPHY_IN**0_2** of the C-PHY primary drive circuit, and control signals CPHY_IP**1_1**, CPHY_IP**1_2**, CPHY_IN**1_1** and CPHY_IN**1_2** of the C-PHY pre-emphasis drive circuit. The primary drive circuit includes two types "T**1**" and "T**2**".

[0044] The drive signal selection module **103** is configured to select an output signal of the C-PHY drive signal generation module and the D-PHY drive signal generation module, where the output signal is used as an input control signal of the multiplex drive module **104** to control each adjustable output resistor to be on and off

[0045] Signals DPHY_IP**0** and DPHY_IN**0** are used to control an output of the primary drive circuit of the multiplex drive module in a D-PHY mode. In a case that DPHY_IP**0** is 1 and DPHY_IN**0** is 0, a high level is outputted by the primary drive circuit of the multiplex drive module. In a case that DPHY_IP**0** is 0 and DPHY_IN**0** is 1, a low level is outputted by the primary drive circuit of the multiplex drive module.

[0046] Signals DPHY_IP**1** and DPHY_IN**1** are used to control an output of the pre-emphasis drive circuit of the multiplex drive module in the D-PHY mode. In a case that DPHY_IP**1** is 1 and DPHY_IN**1** is 0, a high level is outputted by the pre-emphasis drive circuit of the multiplex drive module. In a case that DPHY_IP**1** is 0 and DPHY_IN**1** is 1, a low level is outputted by the pre-emphasis drive circuit of the multiplex drive module.

[0047] Signals CPHY_IP**0_1**, CPHY_IP**0_2**, CPHY_IN**0_1** and CPHY_IN**0_2** are used to control an output of the primary drive circuit of the multiplex drive module in a C-PHY mode. In a case that CPHY_IP**0_1** is equal to 1, CPHY_IP**0_2** is equal to 1, CPHY_IN**0_1** is equal to 0 and CPHY_IN**0_2** is equal to 0, a high level is outputted by the primary drive circuit of the multiplex drive module. In a case that CPHY_IP**0_1** is equal to 0, CPHY_IP**0_2** is equal to 0, CPHY_IN**0_1** is equal to 1 and CPHY_IN**0_2** is equal to 1, a low level is outputted by the primary drive circuit of the multiplex drive module. In a case that CPHY_IP**0_1** is equal to 0, CPHY_IP**0_2** is equal to 0, CPHY_IN**0_1** is equal to 1 and CPHY_IN**0_2** is equal to 0, a high impedance state is outputted by the primary drive circuit of the multiplex drive module. In a case that CPHY_IP**0_1** is equal to 1, CPHY_IP**0_2** is equal to 0, CPHY_IN**0_1** is equal to 1 and CPHY_IN**0_2** is equal to 0, a middle level is outputted by the primary drive circuit of the multiplex drive module.

[0048] Signals CPHY_IP**1_1**, CPHY_IP**1_2**, CPHY_IN**1_1** and CPHY_IN**1_2** are used to control an output of the pre-emphasis drive circuit of the multiplex drive module in the C-PHY mode. In a case that CPHY_IP**1_1** is equal to 1, CPHY_IP**1_2** is equal to 1, CPHY_IN**1_1** is equal to 0 and CPHY_IN**1_2** is equal to 0, a high level is outputted by the pre-emphasis drive circuit of the multiplex drive module. In a case that CPHY_IP**1_1** is equal to 0, CPHY_IP**1_2** is equal to 0, CPHY_IN**1_1** is equal to 1 and CPHY_IN**1_2** is equal to 1, a low level is outputted by the pre-emphasis drive circuit of the multiplex drive module. In a case that CPHY_IP**1_1** is equal to 0, CPHY_IP**1_2** is equal to 0, CPHY_IN**1_1** is equal to 1 and CPHY_IN**1_2** is equal to 0, a high impedance state is outputted by the pre-emphasis drive circuit of the multiplex drive module. In a case that CPHY_IP**1_1** is equal to 1, CPHY_IP**1_2** is equal to 0, CPHY_IN**1_1** is equal to 1 and CPHY_IN**1_2** is equal to 0, a middle level is outputted by the pre-emphasis drive circuit of the multiplex drive module.

[0049] IP**0_1**, IP**0_2**, IN**0_1**, IN**0_2**, IP**1_1**, IP**1_2**, IN**1_1** and IN**1_2** are output signals of the drive signal selection module, and are used to directly control a pull-up resistor and a pull-down resistor of the multiplex drive module to be on and off. In the D-PHY mode, IP**0_1** and IP**0_2** are the same as DPHY_IP**0**, IN**0_1** and IN**0_2** are the same as DPHY_IN**0**, IP**1_1** and IP**1_2** are the same as DPHY_IP**1**, and IN**1_1** and IN**1_2** are the same as DPHY_IN**1**. In the C-PHY mode, IP**0_1**, IP**0_2**, IN**0_1**, IN**0_2**, IP**1_1**, IP**1_2**, IN**1_1** and IN**1_2** are respectively corresponding to CPHY_IP**0_1**, CPHY_IP**0_2**, CPHY_IN**0_1**, CPHY_IN**0_2**, CPHY_IP**1_1**, CPHY_IP**1_2**, CPHY_IN**1_1** and CPHY_IN**1_2**.

[0050] The high speed signal drive circuit according to the embodiment of the present disclosure includes a D-PHY drive signal generation module **101**, a C-PHY drive signal generation module **102**, a drive signal selection module **103** and a multiplex drive module **104**. An output terminal of the D-PHY drive signal generation module **101** and an output terminal of the C-PHY drive signal generation module **102** are both connected to an input terminal of the drive signal selection module **103**. An output terminal of the drive signal selection module **103** is connected to an input terminal of the multiplex drive module **104**. The D-PHY drive signal generation module **101** is configured to generate a D-PHY drive signal, and the C-PHY drive signal generation module **102** is configured to generate a C-PHY drive signal. The drive signal selection module **103** is configured to receive the D-PHY drive signal or the C-PHY drive signal, and control a control switch of the multiplex drive module **104** to be on and off based on the D-PHY drive signal or the C-PHY drive signal, so that the multiplex drive module **104** realizes a function of a D-PHY drive circuit or a C-PHY drive circuit. In this way, dual functions of the D-PHY drive circuit and the C-PHY drive circuit can be realized merely by the high speed signal drive circuit according to the present disclosure.

[0051] Besides, the embodiment of the present disclosure can realize functions of D-PHY without pre-emphasis, D-PHY with pre-emphasis, C-PHY T**1**/T**2** Driver mode and C-PHY with pre-emphasis.

[0052] In an embodiment based on the above embodiment, the multiplex drive module **104** includes at least three drive sub-modules, where each of the at least three drive sub-modules includes eight control switches and eight adjustable output resistors, each of four adjustable output resistors of the eight adjustable output resistors is connected to a termination power supply through a respective one of the eight control switches, each of another four adjustable output resistors of the eight adjustable output resistors is connected to a grounding terminal through a respective one of the eight control switches, and terminals of all the adjustable output resistors, which are not connected to the control switches, are connected to each other to function as an output terminal.

[0053] The structure of the multiplex drive module **104** is described hereinafter taking the multiplex drive module **104** including only three drive sub-modules for example.

[0054] Referring to FIG. **2**, the multiplex drive module **104** includes three drive sub-modules, and each of the three drive sub-modules includes eight adjustable output resistors. For example, in a first drive sub-module, an adjustable output resistor **11** is connected to a termination power supply Vreg through a control switch A_IP**0_1**, an adjustable output resistor **12** is connected to the termination power supply Vreg through a control switch A_IP**0_2**, an adjustable output resistor **13** is connected to the termination power supply Vreg through a control switch A_IP**1_1**, an adjustable output resistor **14** is connected to the termination power supply Vreg through a control switch A_IP**1_2**, an adjustable resistor output **15** is connected to a termination power supply Vss through a control switch A_IN**0_1**, an adjustable output resistor **16** is connected to the termination power supply Vss through a control switch A_IN**0_2**, an adjustable output resistor **17** is connected to the termination power supply Vss

through a control switch A_IN**1**_**1**, and an adjustable output resistor **18** is connected to the termination power supply Vss through a control switch A_IN**1**_**2**. Vreg is a termination power supply generally with a voltage of 400 mV, and the voltage of Vreg may be configured and adjusted by a chip in practical application, which may be implemented by an in-chip LDO (Low Dropout Regulator) generally. The adjustable output resistor **11**, **12**, **13** and **14** may be referred to as pull-up resistors, and the adjustable output resistors **15**, **16**, **17** and **18** may be referred to as pull-down resistors. Resistance values of the adjustable output resistors **11**, **12**, **15** and **16** are the same, and resistance values of the adjustable output resistors **13**, **14**, **17** and **18** are the same.

[0055] Circuit **1** in the first drive sub-modules is a primary drive circuit, and circuit **2** in the first drive sub-modules is a pre-emphasis drive circuit. In order to overcome signal attenuation in a transmission link, certain amplitude is added to a signal within a very first signal period after a polarity of the signal is reversed, which is defined as a pre-emphasis process.

[0056] Terminals of all adjustable output resistors in the first drive sub-module, which are not connected to the control switches, are connected to each other to form an output terminal A_OUT of the first drive sub-module.

[0057] The structure of the other two drive sub-modules are same as that of the first drive sub-module, which is not described again herein for simplicity.

[0058] The multiplex drive module **104** is a multiplex high speed drive circuit including both a D-PHY drive mode and a C-PHY drive mode. The drive signal selection module **103** is configured to select control signals of all switches. For example, in the D-PHY mode, the output signal DPHY_IP**0** of the D-PHY drive signal generation module **101** is sent to two control switches IP**0**_**1** and IP**0**_**2** of the multiplex drive module **104**, the output signal DPHY_IN**0** is sent to two control switches IN**0**_**1** and IN**0**_**2** of the multiplex drive module **104**, the output signal DPHY_IP**1** is sent to two control switches IP**1**_**1** and IP**1**_**2** of the multiplex drive module **104**, and the output signal DPHY_IN**1** is sent to two control switches IN**1**_**1** and IN**1**_**2** of the multiplex drive module **104**.

[0059] In the C-PHY mode, the output signals CPHY_IP**0**_**1**, CPHY_IP**0**_**2**, CPHY_IN**0**_**1** and CPHY_IN**0**_**2** of the C-PHY drive signal generation module **102** are sent to control switches IP**0**_**1**, IP**0**_**2**, IN**0**_**1** and IN**0**_**2** of the multiplex drive module **104** respectively, and the output signals CPHY_IP**1**_**1**, CPHY_IP**1**_**2**, CPHY_IN**1**_**1** and CPHY_IN**1**_**2** of the C-PHY drive signal generation module **102** are sent to control switches IP**1**_**1**, IP**1**_**2**, IN**1**_**1** and IN**1**_**2** of the multiplex drive module **104** respectively. Meanwhile, a C-PHY T**1** diver mode and a C-PHY T**2** driver mode can also be realized.

[0060] In an embodiment based on this embodiment, the adjustable output resistor includes multiple branches connected in parallel, and each of the multiple branches includes multiple resistor branches R that are connected in parallel with each other and a switch K connected in series with all the multiple resistor branches that are connected in parallel with each other. Referring to FIG. **3**, switches of the multiple branches are different from each other, for example, eight resistor branches that are connected in parallel with each other are all connected to switch K**1**.

[0061] FIG. **3** is merely exemplary, and the number of branches may be greater in practical application. In practical application, resistance values of the adjustable output resistors **11** and **12** may be configured based on practical scenarios of application.

[0062] Each adjustable output resistor is turned on and off by a respective switch. For example, control signals of the primary drive circuit are A_IP**0**_**1**, A_IP**0**_**2**, A_IN**0**_**1** and A_IN**0**_**2**, and control signals of the pre-emphasis drive circuit are A_IP**1**_**1**, A_IP**1**_**2**, A_IN**1**_**1** and A_IN**1**_**2**. In a case that a control signal is a logic high level "1", the switch is turned on and the output resistor is functional. In a case that the control signal is a logic low level "0", the switch is off and the output resistor is disconnected.

[0063] In the embodiment, a detailed circuit structure of the multiplex drive module **104** is provided. Therefore, the dual functions of the D-PHY drive circuit and the C-PHY drive circuit can be realized by the multiplex drive module **104** according to the embodiment of the present disclosure.

[0064] In an embodiment based on the embodiment corresponding to FIG. **2**, output terminals of two drive sub-modules in the multiplex drive module **104** are connected to each other through a load resistor in a case that the multiplex drive module **104** is configured to function as a D-PHY drive circuit.

[0065] Referring to FIG. **4**, two drive sub-modules **401** and **402** form a D-PHY drive circuit. Output terminals of the two drive sub-modules are connected to each other through two load resistors, to form a transmission channel, and a third drive sub-module **403** is idle. Control of a D-PHY primary drive circuit and a D-PHY pre-emphasis drive circuit can be realized by turning off control switches. It is noted that the legends **401** to **403** in FIG. **5** designate the same drive sub-modules as in FIG. **4**.

[0066] In an embodiment based on this embodiment, in receiving the D-PHY drive signal or the C-PHY drive signal and controlling the control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, by which the multiplex drive module **104** functions as the D-PHY drive circuit or the C-PHY drive circuit, the drive signal selection module **103** is configured to:

[0067] control, in a case that the D-PHY drive signal is a first primary drive control signal and the C-PHY drive signal is null, a control switch of the multiplex drive module **104** corresponding to the first primary drive control signal to be closed, by which the multiplex drive module **104** functions as the D-PHY drive circuit, where the first primary drive control signal includes a control signal of the D-PHY primary drive circuit and/or a control signal of the D-PHY pre-emphasis drive circuit.

[0068] In a case that the first primary drive control signal includes the control signal of the D-PHY primary drive circuit, the primary drive circuit is controlled. In a case that the first primary drive control signal includes the control signal of the D-PHY primary drive circuit and the control signal of the D-PHY pre-emphasis drive circuit, the pre-emphasis drive circuit is controlled.

[0069] In an embodiment, referring to FIG. **4**, IP**0** and IP**1** represent input control signals of the primary drive circuit, and IP**1** and IN**1** represent input control signals of the pre-emphasis drive circuit. If the D-PHY pre-emphasis is disabled, it means that the first primary drive control signal is the control signal of the D-PHY primary drive circuit. If signals A_IP**0**_**1** and A_IP**0**_**2** are both **1**, two pull-up resistors in channel A are connected to each other, presenting

pull-up characteristics. If signals B_IN**0_1** and B_IN**0_2** are both **1**, two pull-down resistors in channel A are connected to each other, presenting pull-down characteristics. Vreg is 400 mV and a resistance value of the adjustable output resistor **1** is 50 ohm. Calculated by method of division of voltage, a voltage outputted from terminal A_OUT is 300 mV and a voltage outputted from terminal B_OUT is 100 mV.

[0070] As shown in FIG. **4**, RX is composed of two load resistors. RX refers to Receiver PI-W, that is, a data receiving physical interface configured to convert a physical signal to a digital signal for processing by a logic circuit. Other part than RX in FIG. **4** is TX. TX refers to Transmitter PI-W, that is, a data transmitting physical interface configured to convert the digital signal to a physical signal that conforms to an electrical protocol specification.

[0071] Further, reference is made to FIG. **5**, if the D-PHY pre-emphasis is enabled, it means that the first primary drive control signal includes both the control signal of the D-PHY primary drive circuit and the control signal of the D-PT-W pre-emphasis drive circuit.

[0072] For example, the voltage outputted from the terminal A_OUT is 300 mV and the voltage outputted from the terminal B_OUT is 100 mV. A_IP**1_1** and A_IP**1-2** are both turned on at the same time, and the pull-up capability of the terminal A_OUT is improved. B_IN**1_1** and B_IN**1_2** are both turned on at the same time, and the pull-down capability of the terminal B_OUT is improved. By setting a resistance value of the adjustable output resistor **2** and connecting the adjustable output resistor **2** in parallel with the adjustable output resistor **1**, a higher output amplitude can be obtained than in a case of only using the primary drive circuit.

[0073] Regarding the pre-emphasis process, the amplitude is added to an output signal within a very first period after a polarity of the signal is reversed. Table 1 shows logic levels of signals IP**1_1**, IP**1_2**, IN**1_1** and IN**1_2** obtained based on control logic levels of signal IP**0_1** in two successive periods. In the table, IP**0_1** represents output data. If a polarity of the output data in a next period is reversed compared to a polarity of the output data in the present period, output amplitude of the output data in the next period is increased by a pre-emphasis circuit.

TABLE 1

Truth table of control signals with D-PHY pre-emphasis enabled

Current Period	Next Period				
IP0_1	IP0_1	IP1_1	IN1_1	IP1_2	IN1_2
0	0	0	0	0	0
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

[0074] In an embodiment based on this embodiment, each two drive sub-modules function as an output channel of the D-PHY drive circuit, to realize multiple outputs of the D-PHY drive circuit.

[0075] In an embodiment, the number of the drive sub-modules may be ten.

[0076] A complete D-PHY output interface includes five channels in total, one clock channel and four data channels, that is, ten output ports. The ten output ports are named A, B, C, D, E, F, G, H, I and J for convenience of description. When the interface is used as a D-PHY interface, A and B form an output channel, similarly, C and D, E and F, G and H, I and J form four output channels respectively, that is, five output channels AB, CD, EF, GH and IJ are formed in total.

[0077] In this embodiment, a control process of the multiplex drive module **104** being used as the D-PHY drive circuit is described, and thereby the multiplex drive module **104** can be used according to the control process described in the embodiment.

[0078] In an embodiment based on the embodiment corresponding to FIG. **2**, when the multiplex drive module **104** functions as the C-PHY drive circuit, output terminals of three drive sub-modules of the multiplex drive module **104** are connected to each other in a star connection through a load resistor.

[0079] Referring to FIG. **6**, an output terminal of each drive sub-module is connected to a load resistor, and three load resistors are connected to each other in a star connection, where the three drive sub-modules form a transmission channel. The C-PHY interface has two drive modes, that is, a C-PHY primary drive circuit control mode and a C-PHY pre-emphasis drive circuit control mode, which are described hereinafter.

[0080] In receiving the D-PHY drive signal or the C-PHY drive signal and controlling the control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, by which the multiplex drive module **104** functions as the D-PHY drive circuit or the C-PHY drive circuit, the drive signal selection module **103** is configured to:

[0081] control, in a case that the C-PHY drive signal is a second primary drive control signal and the D-PHY drive signal is null, a control switch of the multiplex drive module **104** corresponding to the second primary drive control signal to be closed, by which the multiplex drive module **104** functions as the C-PHY drive circuit, where the second primary drive control signal includes a control signal of the C-PHY primary drive circuit and/or a control signal of the C-PHY pre-emphasis drive circuit.

[0082] In a case that the second primary drive control signal includes the control signal of the C-PHY primary drive circuit, the primary drive circuit is controlled. In a case that the second primary drive control signal includes both the control signal of the C-PHY primary drive circuit and the control signal of the C-PHY pre-emphasis drive circuit, the pre-emphasis drive circuit is controlled.

[0083] In an embodiment, in the C-PHY specification, the primary drive circuit includes two types of structures T**1** and T**2**.

[0084] Referring to FIG. **6**, a C-PHY primary drive circuit in mode T**1** is shown, that is, a C-PHY primary drive circuit with structure T**1**. Reference is made to Table 2, which shows how to control states of control switches in each channel.

TABLE 2

Truth table of control signals of first C-PHY primary drive circuit

	control											
state	A_IP0_1	A_IN0_1	A_IP0_2	A_IN0_2	B_IP0_1	B_IN0_1	B_IP0_2	B_IN0_2	C_IP0_1	C_IN0_1	C_IP0_2	C_IN0_2
+X	1	0	1	0	0	1	0	1	0	0	0	0
+Y	0	0	0	0	1	0	1	0	0	1	0	0
+Z	0	1	0	1	0	0	0	0	1	0	1	0
−X	0	1	0	1	1	0	1	0	0	0	0	0
−Y	0	0	0	0	0	1	0	1	1	0	1	0
−Z	1	0	1	0	0	0	0	0	0	1	0	1

[0085] Reference is made to FIG. **7**, which shows a C-PHY primary drive circuit in mode T**2**, that is, a C-PHY primary drive circuit with structure T**2**. Reference is made to Table 3, which shows how to control states of control switches in each channel.

TABLE 3

Truth table of control signals of second C-PHY primary drive circuit

	control											
state	A_IP0_1	A_IN0_1	A_IP0_2	A_IN0_2	B_IP0_1	B_IN0_1	B_IP0_2	B_IN0_2	C_IP0_1	C_IN0_1	C_IP0_2	C_IN0_2
+X	1	0	1	0	0	1	0	1	1	1	0	0
+Y	1	1	0	0	1	0	1	0	0	1	0	1
+Z	0	1	0	1	1	1	0	0	1	0	1	0
−X	0	1	0	1	1	0	1	0	1	1	0	0
−Y	1	1	0	0	0	1	0	1	1	0	1	0
−Z	1	0	1	0	1	1	0	0	0	1	0	1

[0086] Reference is made to FIG. **8**, which shows a C-PHY pre-emphasis drive control circuit. The pre-emphasis process in state "−Z" is shown in FIG. **8**. Two pull-up resistors in the primary drive circuit corresponding to port A are turned on, which is defined as state "H". Two output resistors in the pre-emphasis drive circuit corresponding to port A are turned on and pull up, and in this case, the pull-up driving capability of the primary drive circuit and the pre-emphasis drive circuit corresponding to port A reaches maximum, which is defined as state "H**2**". In a case that one pull-up resistor and one pull-down resistor of the pre-emphasis drive circuit are turned on at the same time, the pull-up driving capability of port A is less than that of state "H**2**", which is defined as state "H**1**". In a case that two pull-down resistors of the pre-emphasis drive circuit are turned on at the same time to pull down, the pull-up driving capability of port A is less than that of state "H**1**", which is defined as state "H**0**".

[0087] Similarly, one output resistor pulls up and one output resistor pulls down in the primary drive circuit corresponding to port B, thereby pull each other, which is defined as state "M". Three states "M**1**+", "M**0**" and "M**1**−" may be formed by combination with different states of the pre-emphasis drive circuit.

[0088] Two output resistors in the primary drive circuit corresponding to port C pull down, which is defined as state "L". Three states "L**0**", "L**1**" and "L**2**" may be formed by combination with different states of the pre-emphasis drive circuit.

[0089] The above definitions of states "H", "M" and "L" also apply to the pre-emphasis drive circuit.

TABLE 4

Truth table of control signals of C-PHY pre-emphasis drive circuit

Control signal of primary drive circuit in a period				Control signal of pre-emphasis drive circuit in a next period			
IP0_1	IN0_1	IP0_2	IN0_2	IP1_1	IN1_1	IP1_2	IN1_2
1	0	1	0	0	1	0	1
1	1	0	0	1	1	0	0
0	1	0	1	1	0	1	0

[0090] Table 4 shows that an output state of a pre-emphasis drive circuit in a next period is determined by a state of a primary drive circuit in a previous period. Control signals of the primary drive circuit shown in Table 4 represent three

states, that is, state "H" in which two pull-up resistors are turned on, state "M" in which one pull-up resistor and one pull-down resistor are turned on, and state "L" in which two pull-down resistors are turned on.

[0091] Resistance values of the adjustable output resistor **1** in the primary drive circuit and the adjustable output resistor **2** in the pre-emphasis drive circuit may be adjusted. Referring to the above description of the operating principle of the pre-emphasis drive circuit, different signal output amplitudes and signal pre-emphasis intensities can be obtained by combination of resistors with different resistance values.

[0092] In an embodiment based on this embodiment, each three of the drive sub-modules function as an output channel of the C-PHY drive circuit, to realize the multiple outputs of the C-PHY drive circuit.

[0093] In an embodiment, there are ten drive sub-modules and accordingly ten output ports. The ten output ports are named A, B, C, D, E, F, G, H, I and J for convenience of description. When the interface is used as a C-PHY interface, A, B and C form an output channel, similarly, D, E and F form an output channel, G, H and I form an output channel, that is, three complete output channels ABC, DEF, GHI are formed, where port J is not in use.

[0094] In this embodiment, a control process of the multiplex drive module **104** being used as the D-PHY drive circuit is described, and thereby the multiplex drive module **104** can be used according to the control process described in the embodiments.

[0095] Based on the above description of the disclosed embodiments, those skilled in the art are capable of carrying out or using the present disclosure. It is obvious for those skilled in the art to make many modifications to these embodiments. The general principle defined herein may be implemented in other embodiments without departing from the spirit or scope of the present application. Therefore, the present invention is not limited to the embodiments illustrated herein, but should be defined by the broadest scope consistent with the principle and novel features disclosed herein.

1. A high speed signal drive circuit, comprising:

a D-PHY drive signal generation module, a C-PHY drive signal generation module, a drive signal selection module and a multiplex drive module,

wherein an output terminal of the D-PHY drive signal generation module and an output terminal of the C-PHY drive signal generation module are both connected to an input terminal of the drive signal selection module, and an output terminal of the drive signal selection module is connected to an input terminal of the multiplex drive module;

the D-PHY drive signal generation module is configured to generate a D-PHY drive signal;

the C-PHY drive signal generation module is configured to generate a C-PHY drive signal; and

the drive signal selection module is configured to: receive the D-PHY drive signal or the C-PHY drive signal, and control a control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, whereby the multiplex drive module function as a D-PHY drive circuit or a C-PHY drive circuit.

2. The high speed signal drive circuit according to claim **1**, wherein the multiplex drive module comprises at least three drive sub-modules;

each of the at least three drive sub-modules comprises eight control switches and eight adjustable resistors, each of four adjustable output resistors of the eight adjustable output resistors is connected to a termination power supply through a respective one of the eight control switches, each of another four adjustable output resistors of the eight adjustable output resistors is connected to a grounding terminal through a respective one of the eight control switches, and terminals of all the adjustable output resistors, which are not connected to the control switches, are connected to each other to function as an output terminal.

3. The high speed signal drive circuit according to claim **2**, wherein in a case that the multiplex drive module is configured to function as the D-PHY drive circuit, output terminals of two drive sub-modules of the at least three drive sub-modules of the multiplex drive module are connected to each other through a load resistor.

4. The high speed signal drive circuit according to claim **2**, wherein in a case that the multiplex drive module is configured to function as the C-PHY drive circuit, output terminals of three drive sub-modules of the at least three drive sub-modules are connected to each other in a star connection through a load resistor.

5. The high speed signal drive circuit according to claim **3**, wherein in receiving the D-PHY drive signal or the C-PHY drive signal and controlling the control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, whereby the multiplex drive module functions as the D-PHY drive circuit or the C-PHY drive circuit, the drive signal selection module is configured to:

control, in a case that the D-PHY drive signal is a first primary drive control signal and the C-PHY drive signal is null, a control switch of the multiplex drive module corresponding to the first primary drive control signal to be closed, whereby the multiplex drive module functions as the D-PHY drive circuit,

wherein the first primary drive control signal comprises a control signal of a D-PHY primary drive circuit and/or a control signal of a D-PHY pre-emphasis drive circuit.

6. The high speed signal drive circuit according to claim **4**, wherein in receiving the D-PHY drive signal or the C-PHY drive signal and controlling the control switch of the multiplex drive module to be on and off based on the D-PHY drive signal or the C-PHY drive signal, whereby the multiplex drive module functions as the D-PHY drive circuit or the C-PHY drive circuit, the drive signal selection module is configured to:

control, in a case that the C-PHY drive signal is a second primary drive control signal and the D-PHY drive signal is null, a control switch of the multiplex drive module corresponding to the second primary drive control signal to be closed, whereby the multiplex drive module functions as the C-PHY drive circuit,

wherein the second primary drive control signal comprises a control signal of a C-PHY primary drive circuit and/or a control signal of a C-PHY pre-emphasis drive circuit.

7. The high speed signal drive circuit according to claim **2**, wherein each two drive sub-modules of the at least three

drive sub-modules function as an output channel of the D-PHY drive circuit, to realize multiple outputs of the D-PHY drive circuit.

8. The high speed signal drive circuit according to claim **2**, wherein each three drive sub-modules of the at least three drive sub-modules function as an output channel of the C-PHY drive circuit, to realize multiple outputs of the C-PHY drive circuit.

9. The high speed signal drive circuit according to claim **2**, wherein the adjustable output resistor comprises a plurality of branches connected in parallel, and each of the plurality of branches comprises a plurality of resistor branches that are connected in parallel with each other and a switch connected in series with all the plurality of resistor branches that are connected in parallel with each other.

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