US 20200243760A1

(19) **United States**
(12) **Patent Application Publication**
Mani
(10) **Pub. No.: US 2020/0243760 A1**
(43) **Pub. Date: Jul. 30, 2020**

(54) **SELF CONTACTING BIT LINE TO MRAM CELL**

(71) Applicant: **III Holdings 1, LLC**, Wilmington, DE (US)

(72) Inventor: **Krishnakumar Mani**, San Jose, CA (US)

(21) Appl. No.: **16/826,498**

(22) Filed: **Mar. 23, 2020**

Related U.S. Application Data

(60) Continuation of application No. 14/886,370, filed on Oct. 19, 2015, now Pat. No. 10,608,171, which is a division of application No. 13/444,805, filed on Apr. 11, 2012, now abandoned.

(60) Provisional application No. 61/473,921, filed on Apr. 11, 2011.

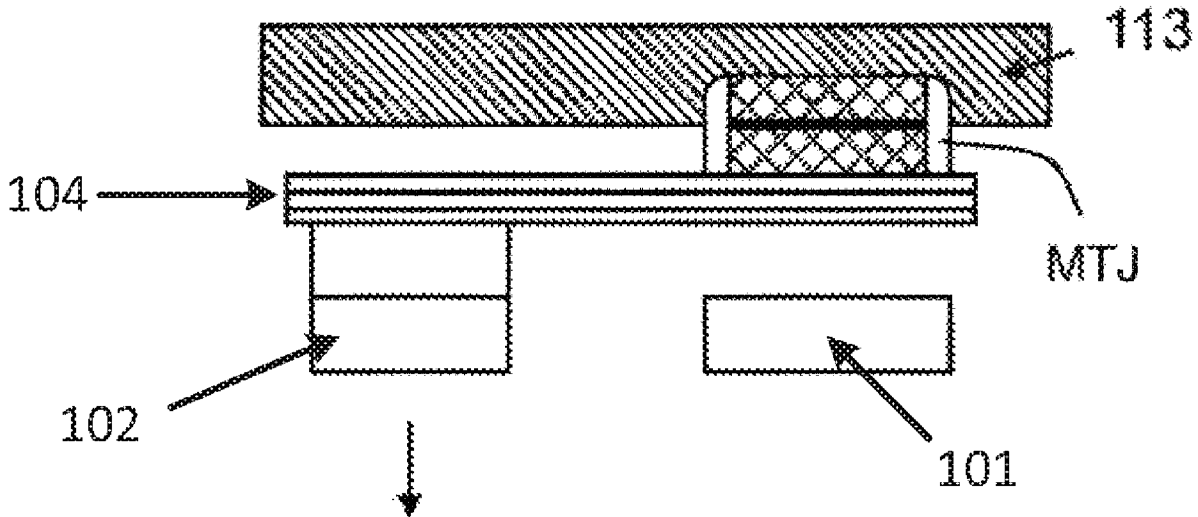
Publication Classification

(51) **Int. Cl.**
H01L 43/12 (2006.01)
G11C 11/16 (2006.01)
H01L 43/08 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 43/12*** (2013.01); *H01L 27/222* (2013.01); ***H01L 43/08*** (2013.01); ***G11C 11/161*** (2013.01)

(57) **ABSTRACT**

Embodiments of the invention disclose magnetic memory cell configurations in which a magnetic storage structure is coupled to an upper metal layer with minimal overlay margin. This greatly reduces a size of the memory cell.



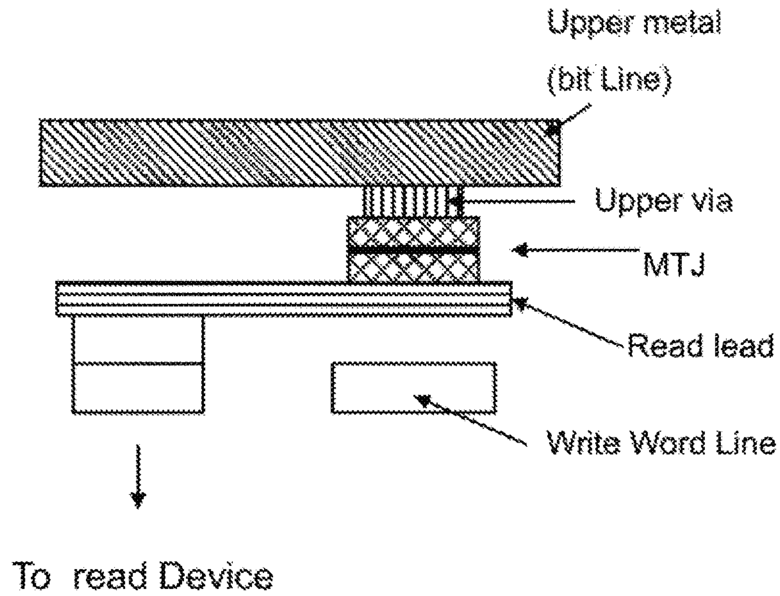
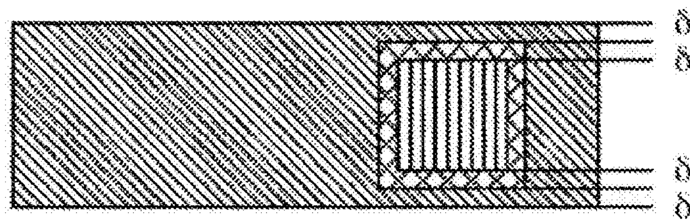


FIG. 1A
Prior Art



MTJ size = f + 2δ
Top metal width = f +4δ
f: Minimum feature size
δ: Overlay Margin

FIG. 1B
Prior Art

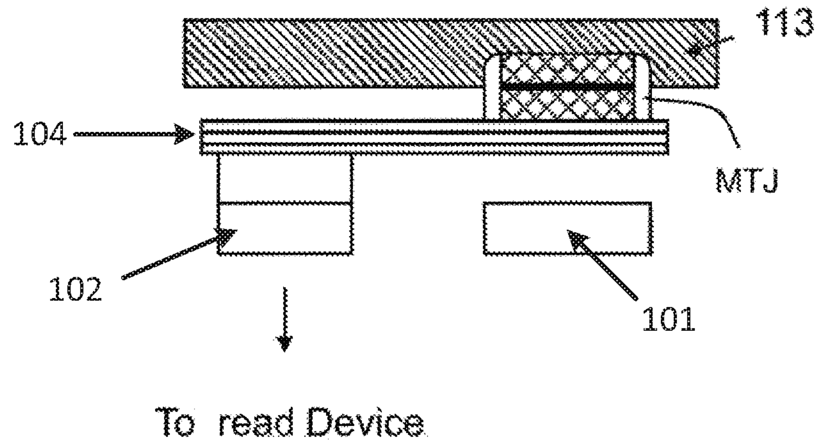
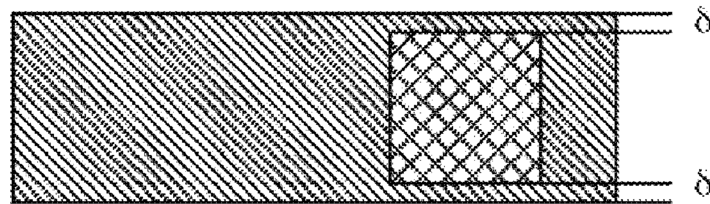


FIG. 2A



MTJ size = f

Top metal width = f +2δ

f: Minimum feature size

δ: Overlay Margin

FIG. 2B

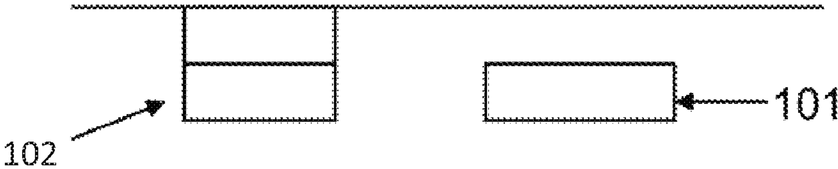


FIG. 3A

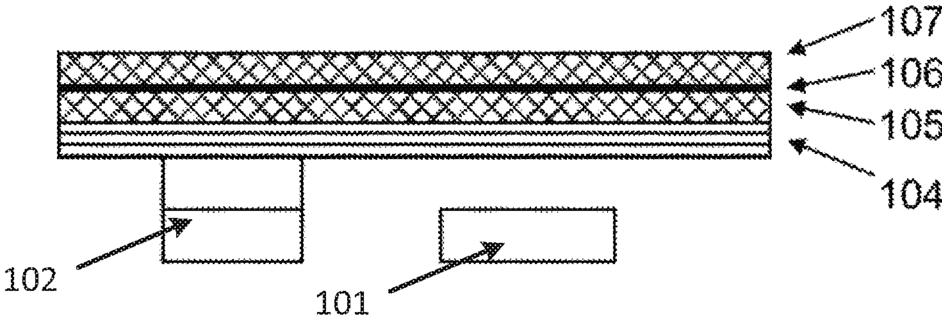


FIG. 3B

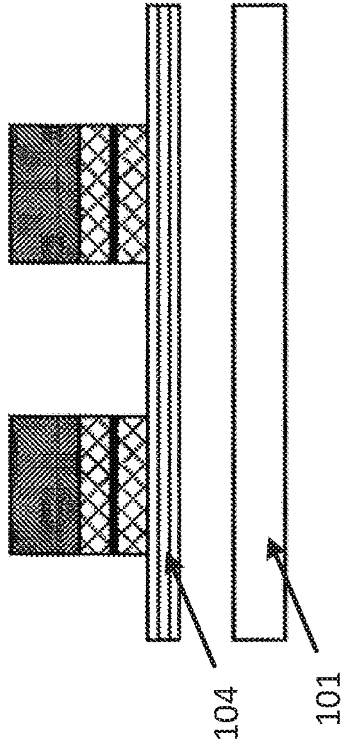


FIG. 4A

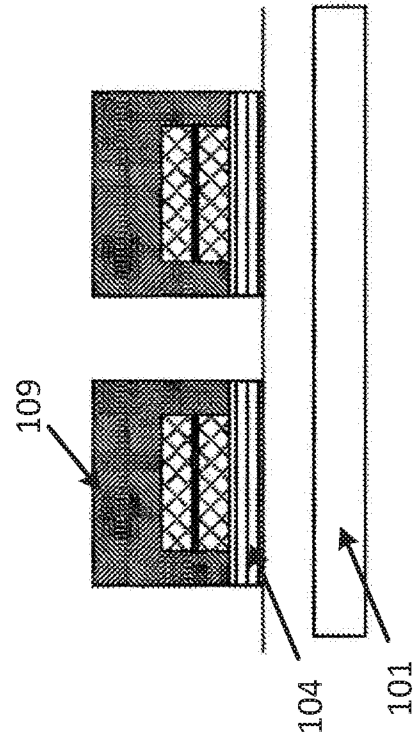


FIG. 4B

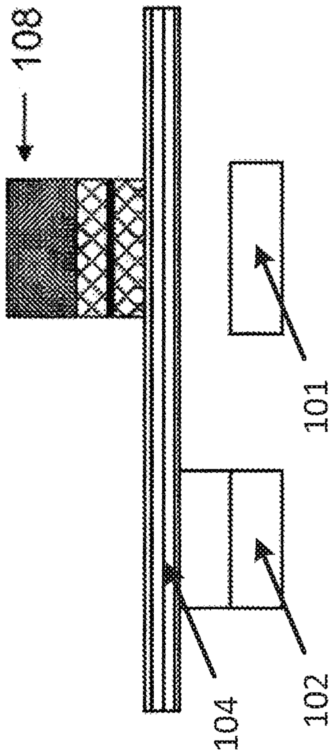


FIG. 3C

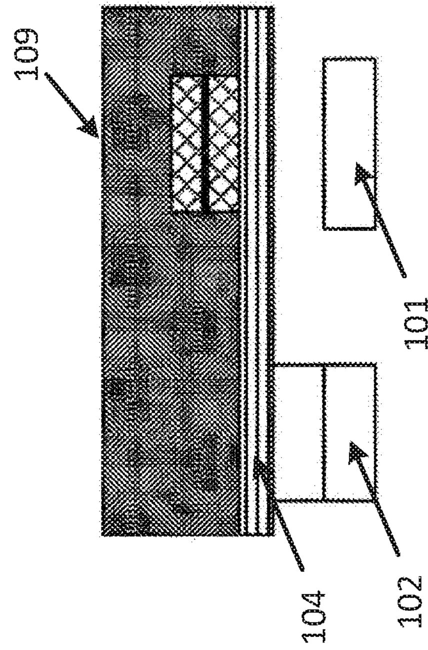


FIG. 3D

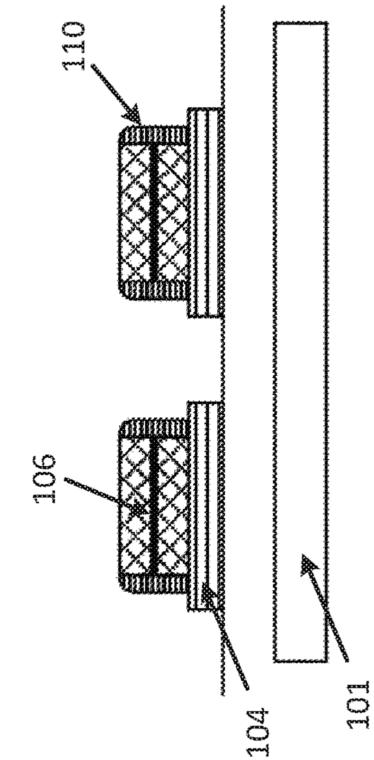


FIG. 4C

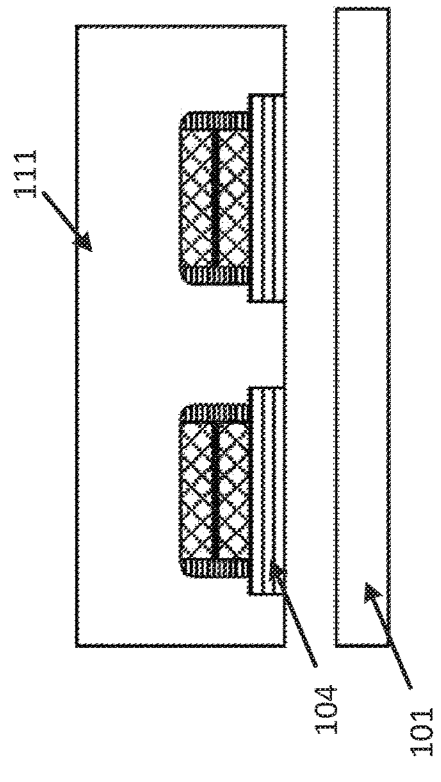


FIG. 4D

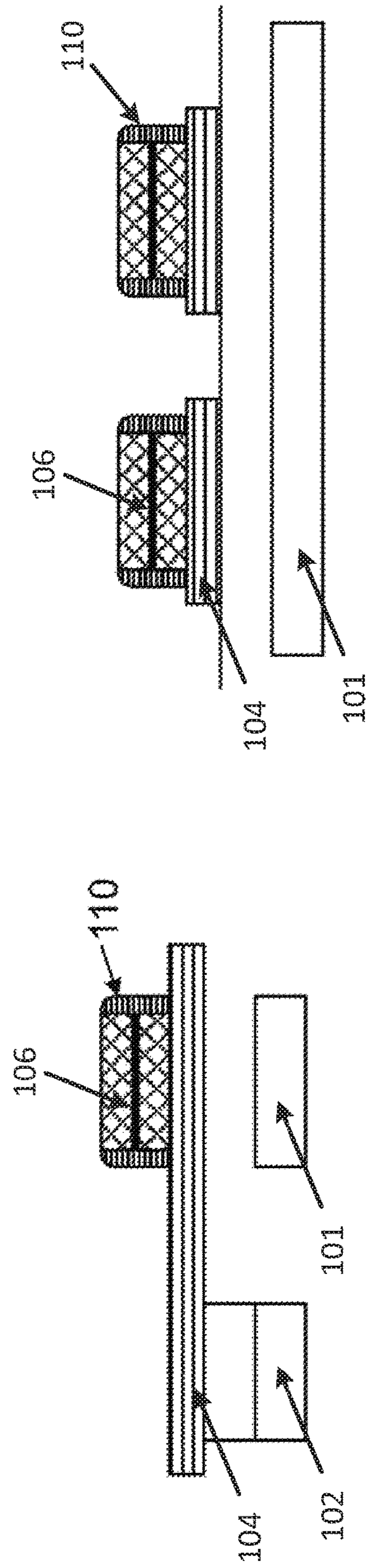


FIG. 3E

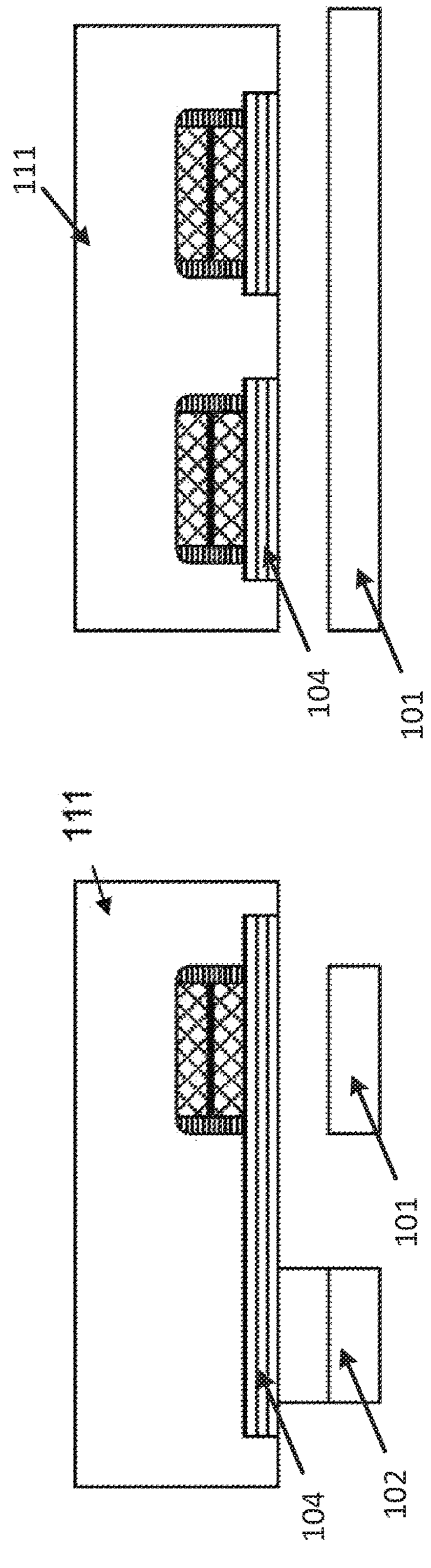


FIG. 3F

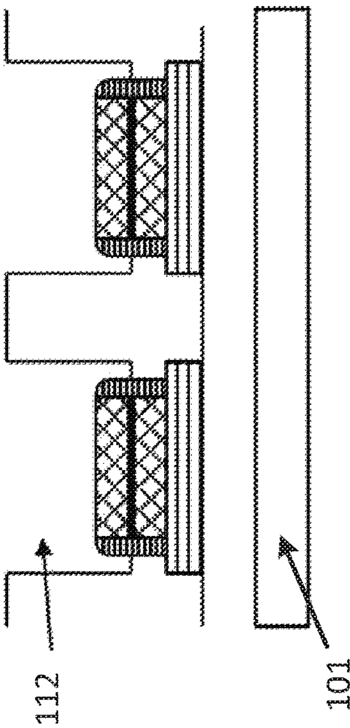


FIG. 4E

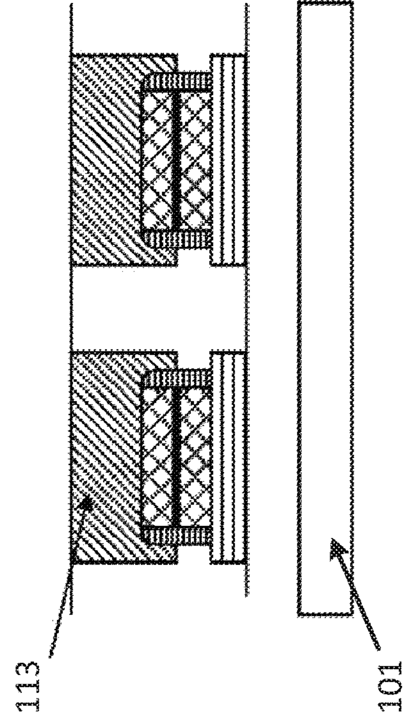


FIG. 4F

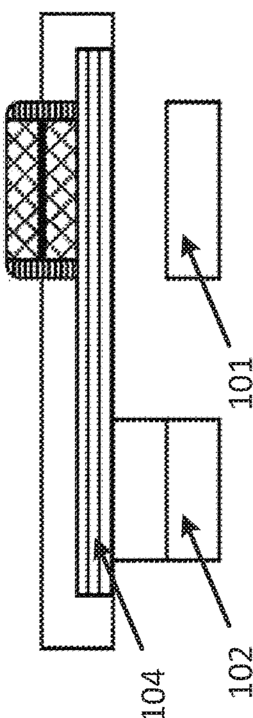


FIG. 3G

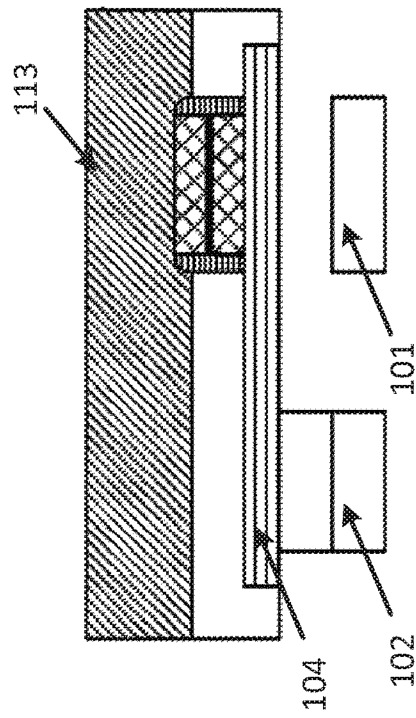


FIG. 3H

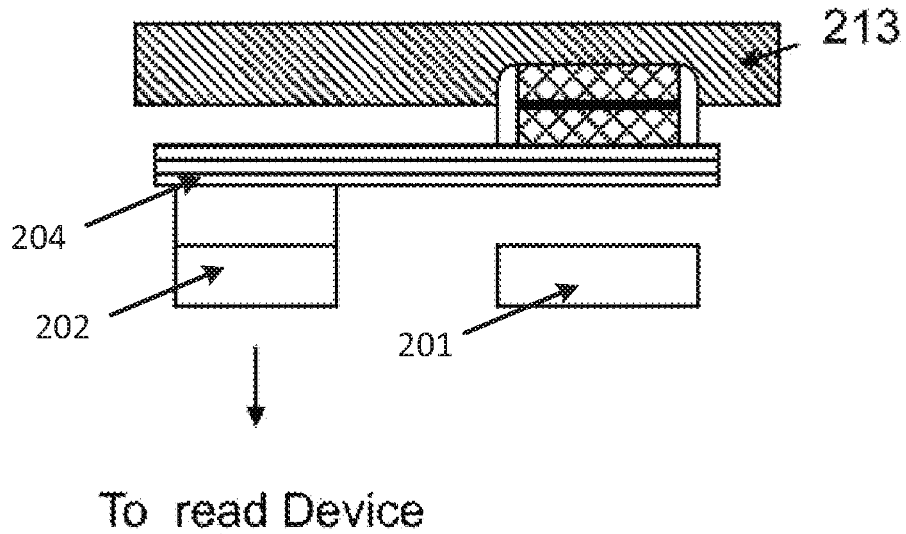


FIG. 5A

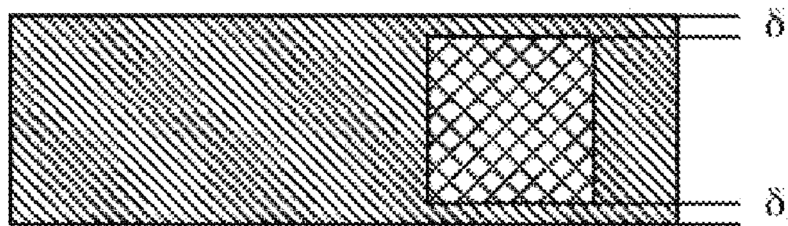


FIG. 5B

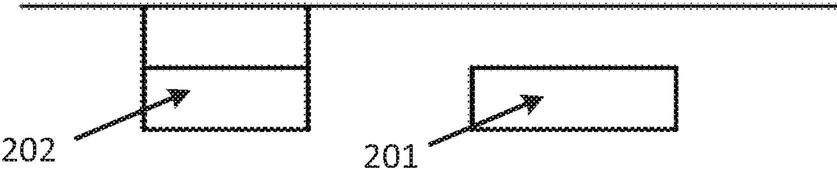


FIG. 6A

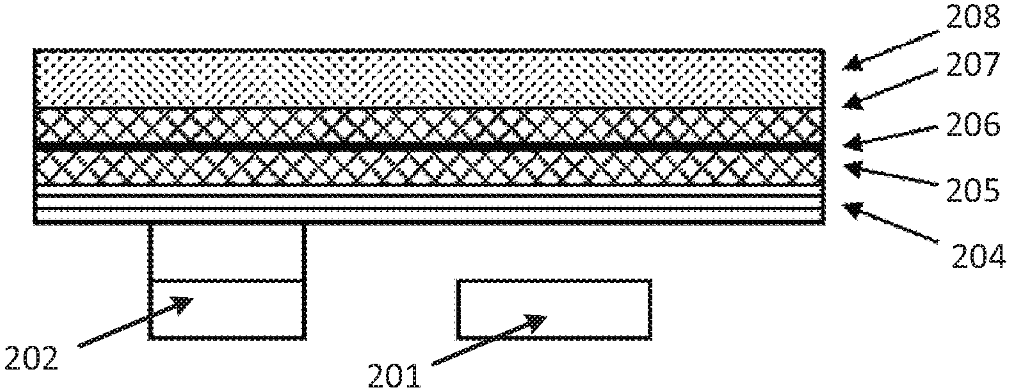


FIG. 6B

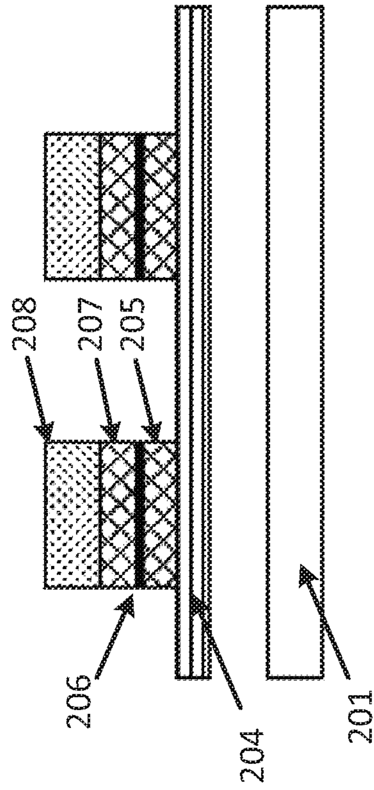


FIG. 7A

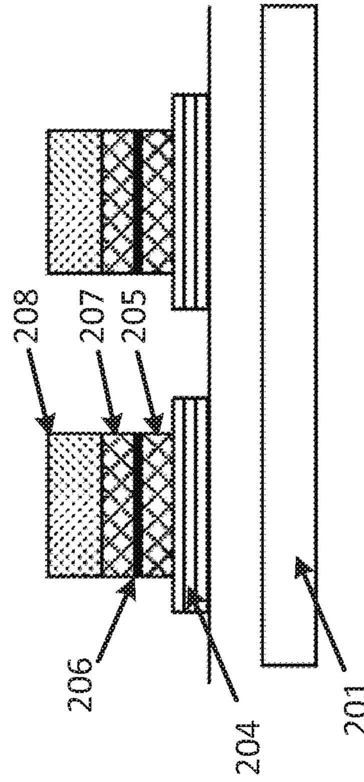


FIG. 7B

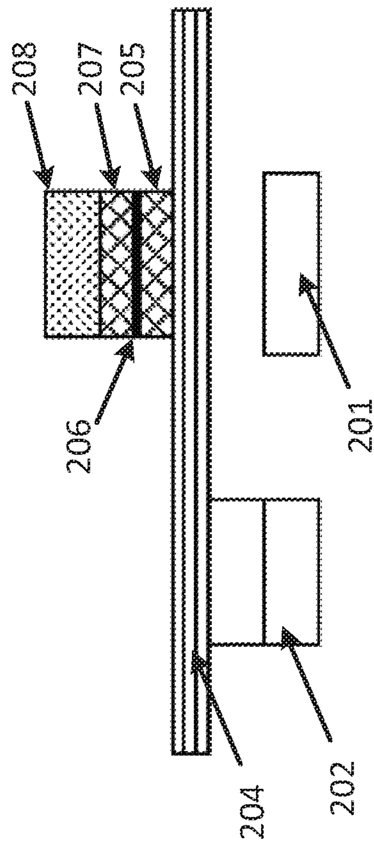


FIG. 6C

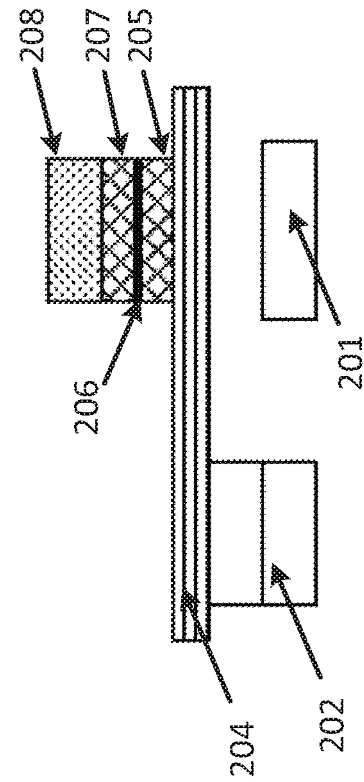


FIG. 6D

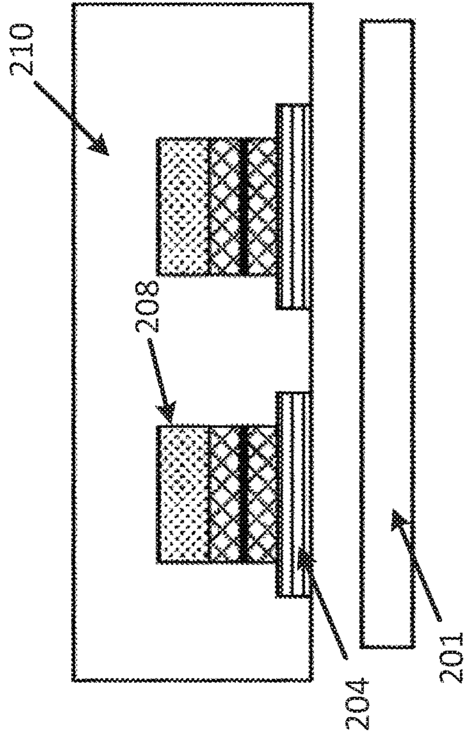


FIG. 7C

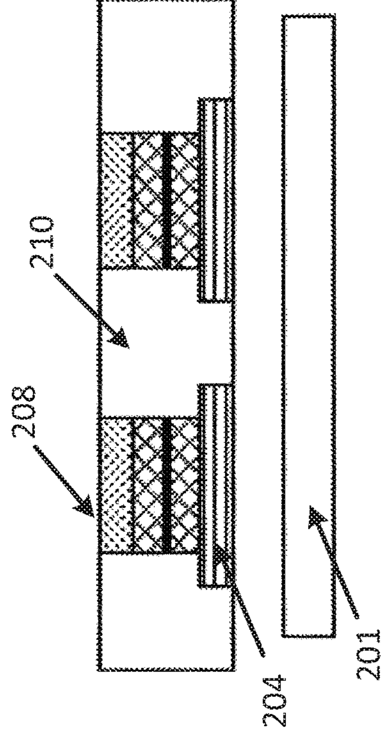


FIG. 7D

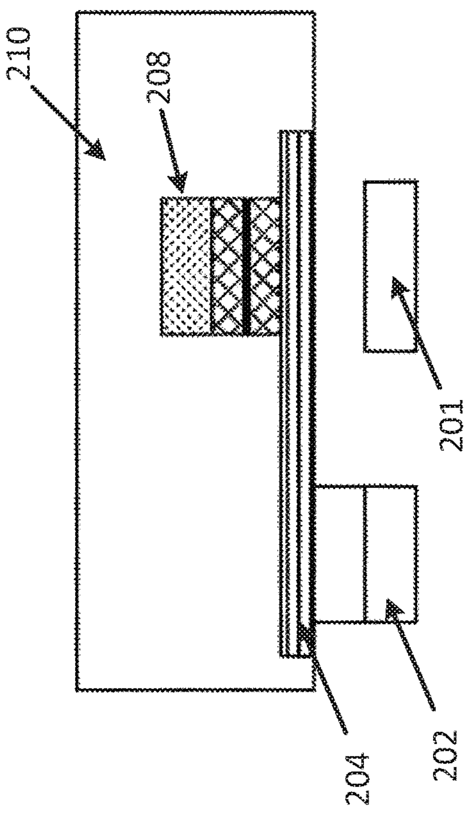


FIG. 6E

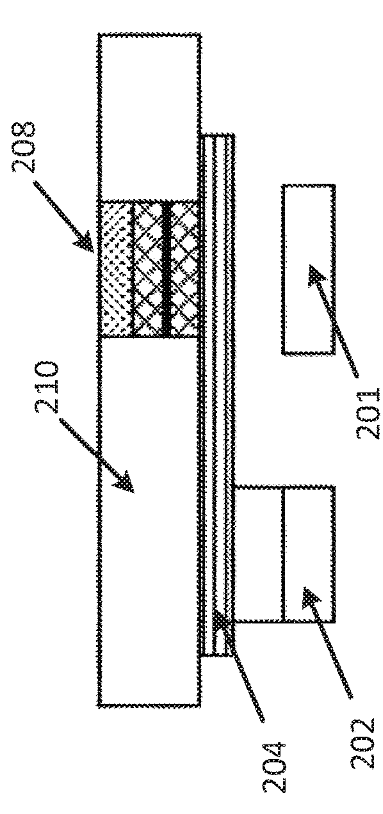


FIG. 6F

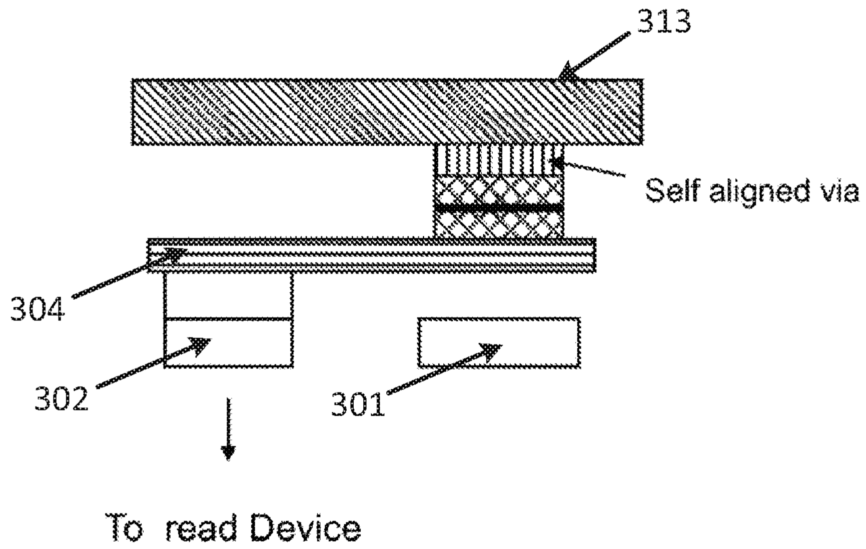
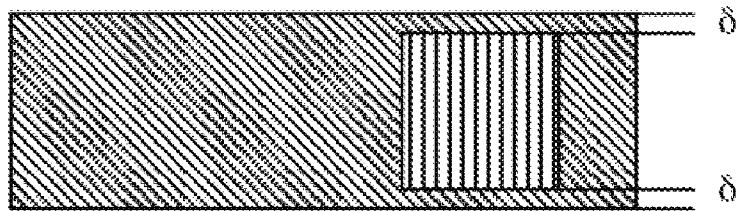


FIG. 8A



MTJ size = f

Top metal width = f +2δ

f: Minimum feature size

δ: Overlay Margin

FIG. 8B

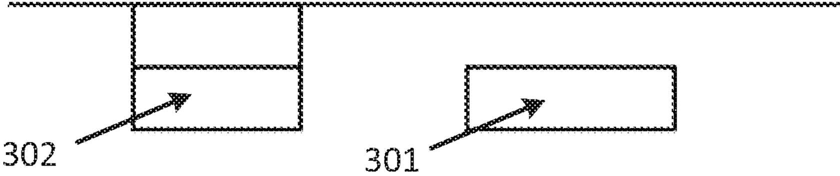


FIG. 9A

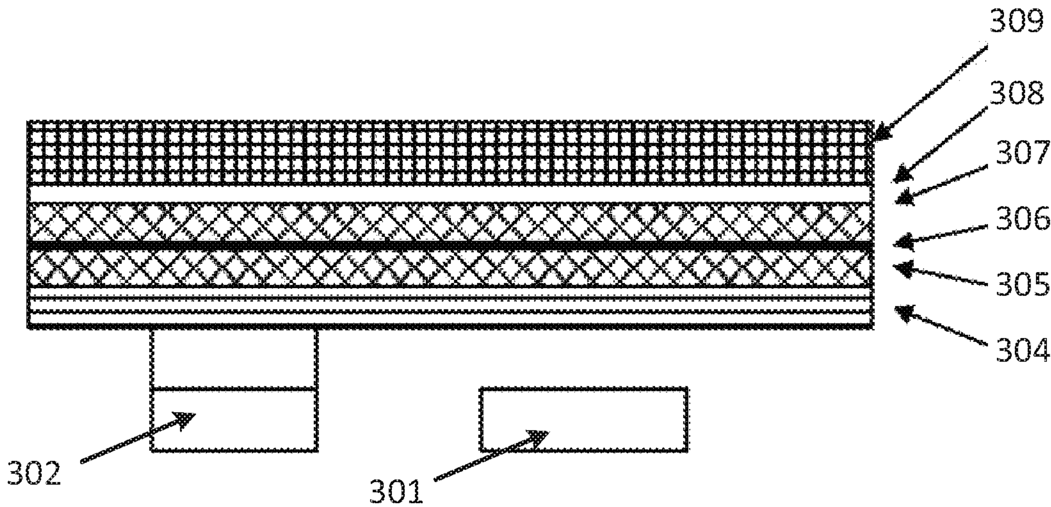


FIG. 9B

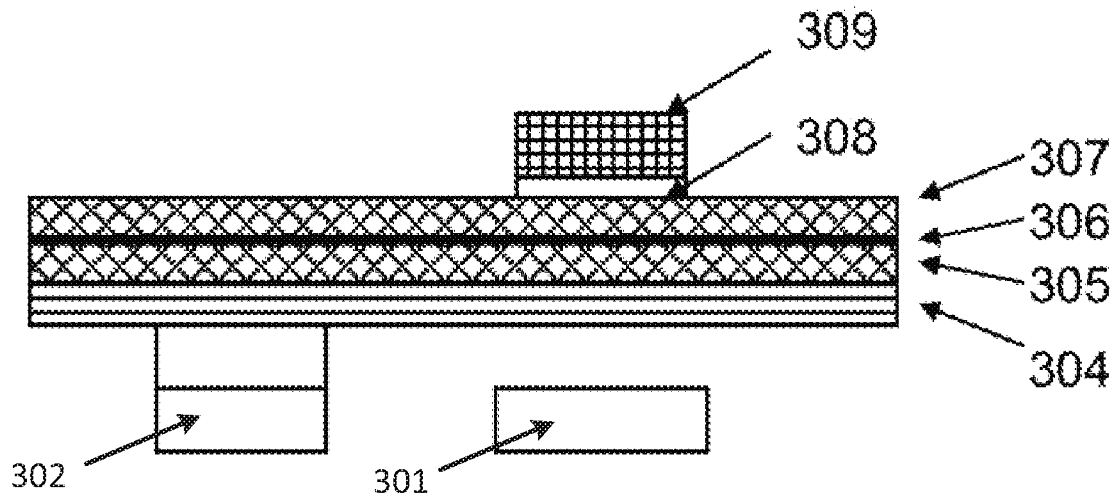


FIG. 9C

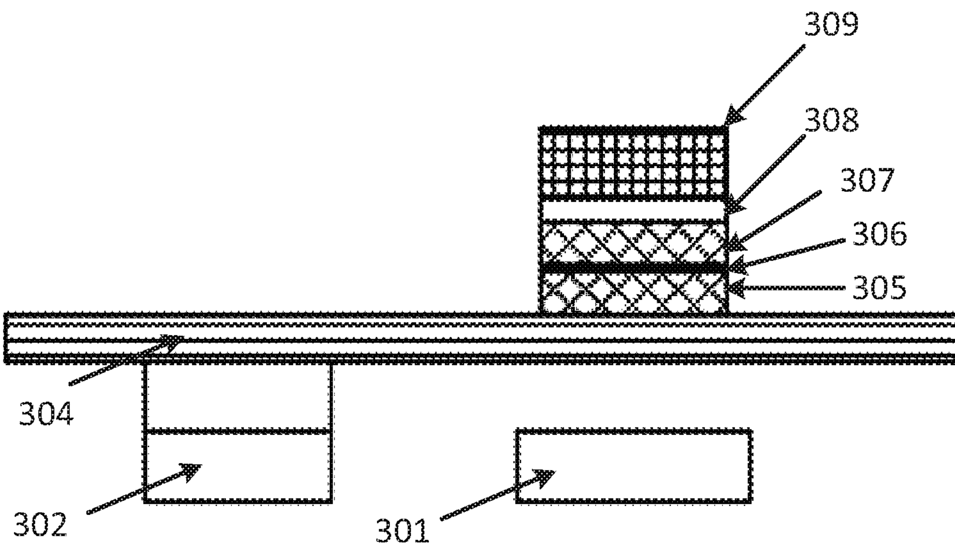


FIG. 9D

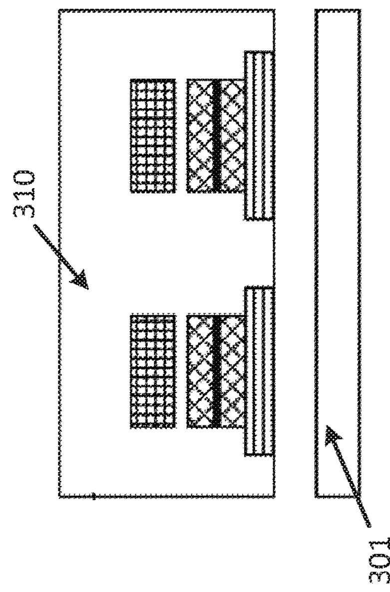


FIG. 10A

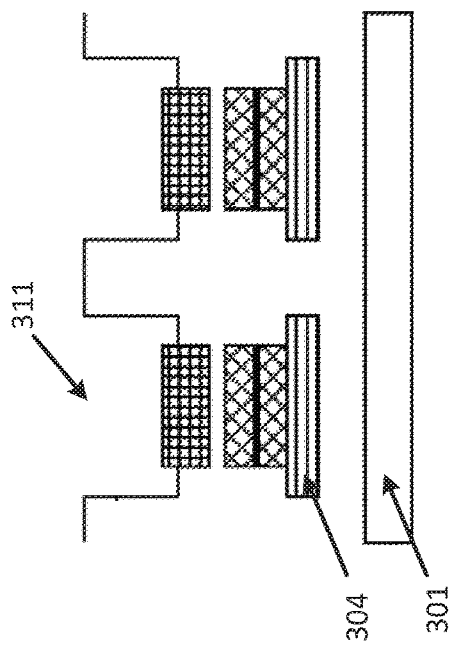


FIG. 10B

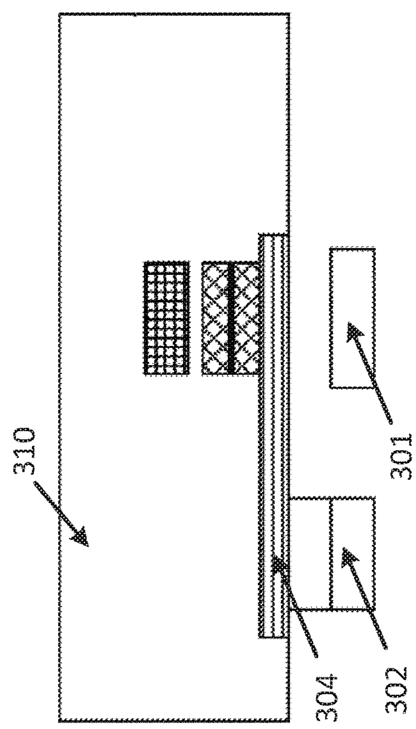


FIG. 9E

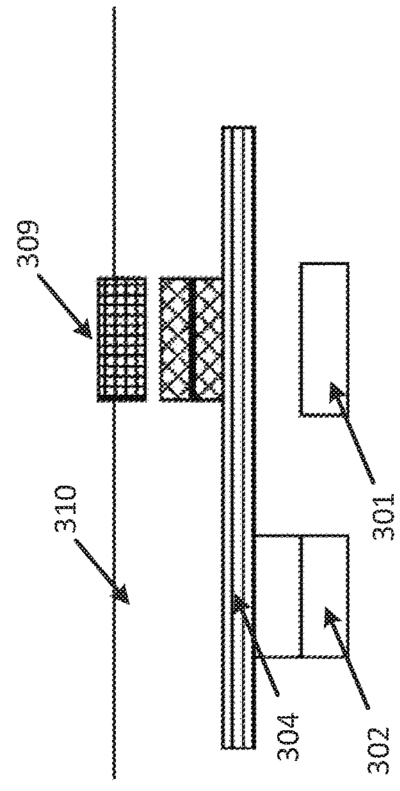
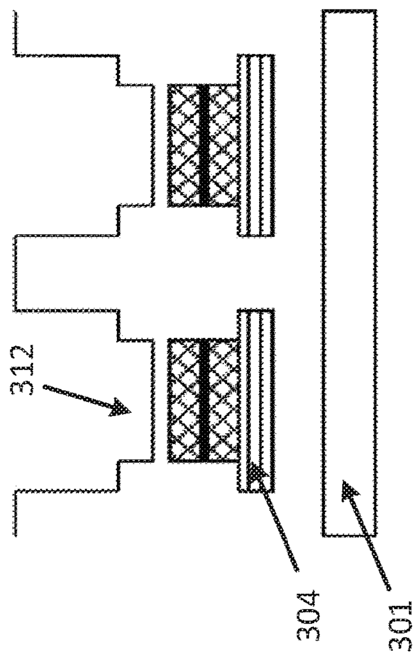


FIG. 9F



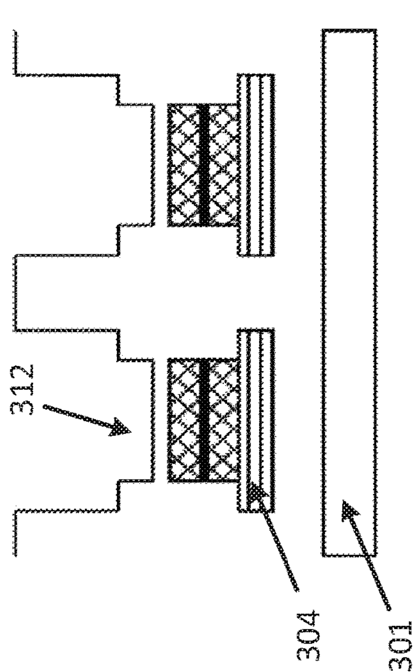


FIG. 10C

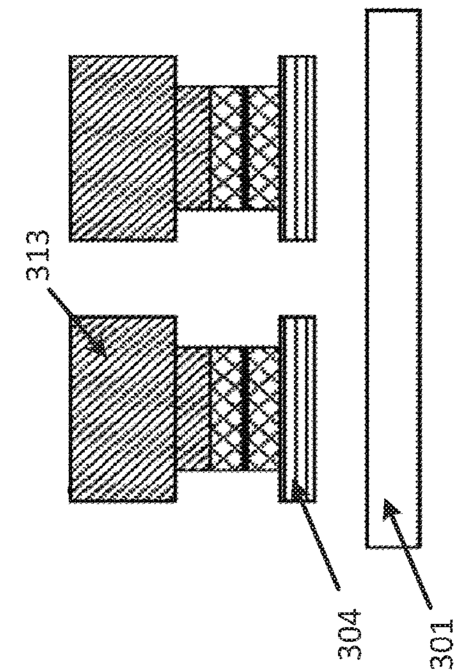


FIG. 10D

FIG. 9G

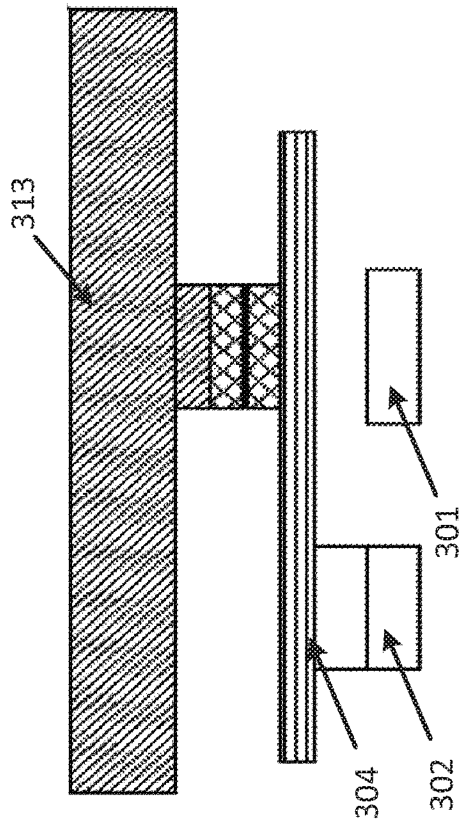


FIG. 9H

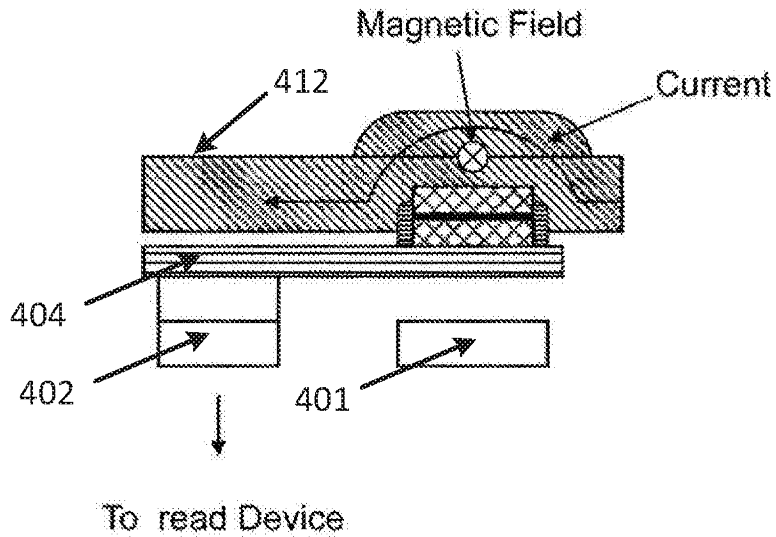
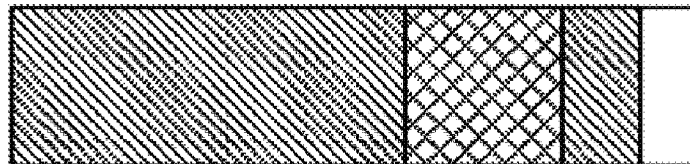


FIG. 11A



MTJ size = f

Top metal width = f

f: Minimum feature size

δ: Overlay Margin

FIG. 11B

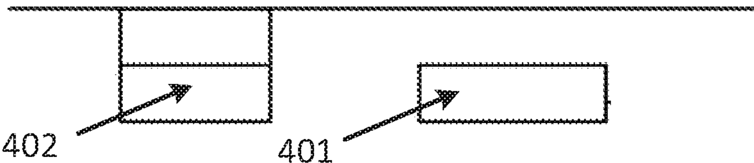


FIG. 12A

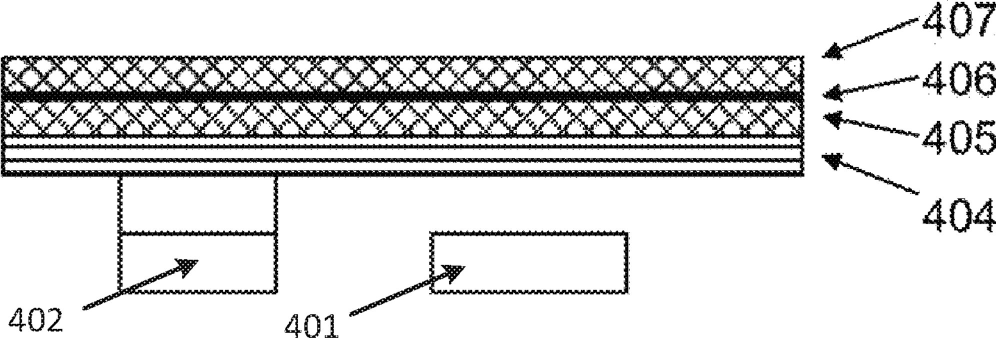


FIG. 12B

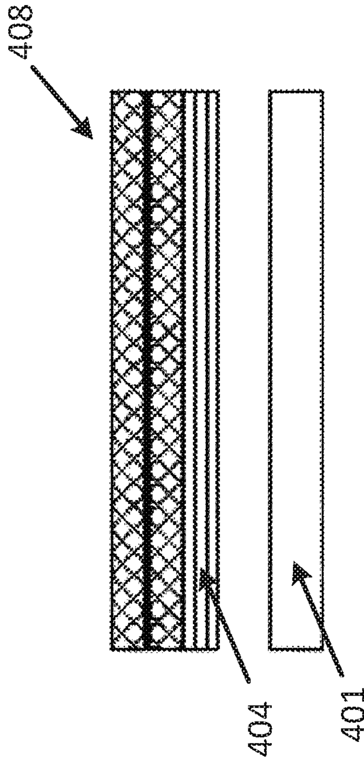


FIG. 13A

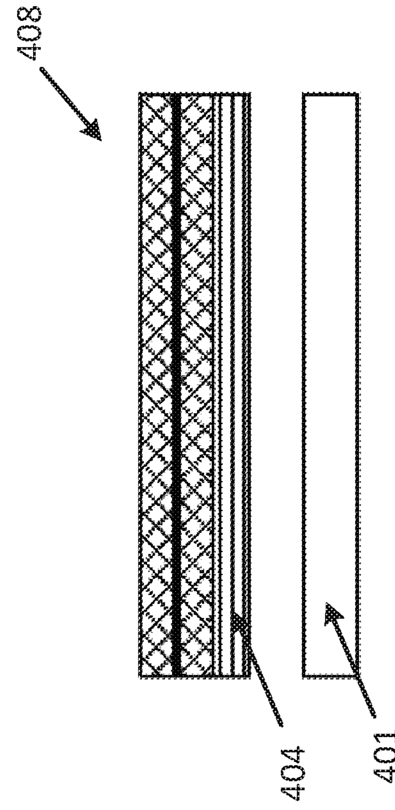


FIG. 13B

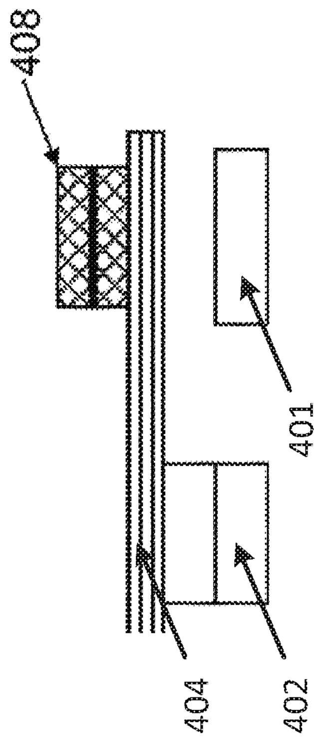


FIG. 12C

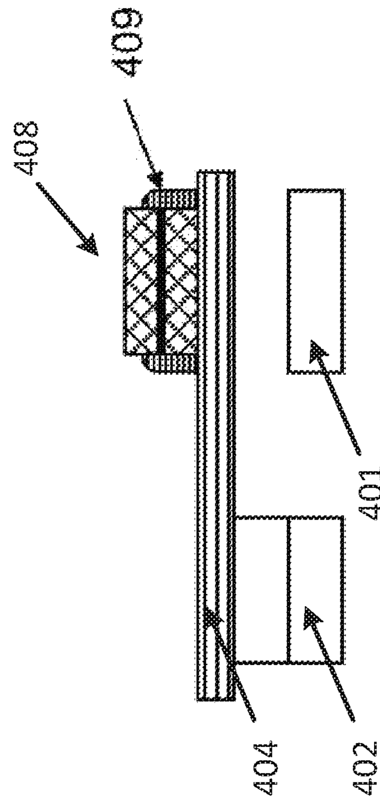


FIG. 12D

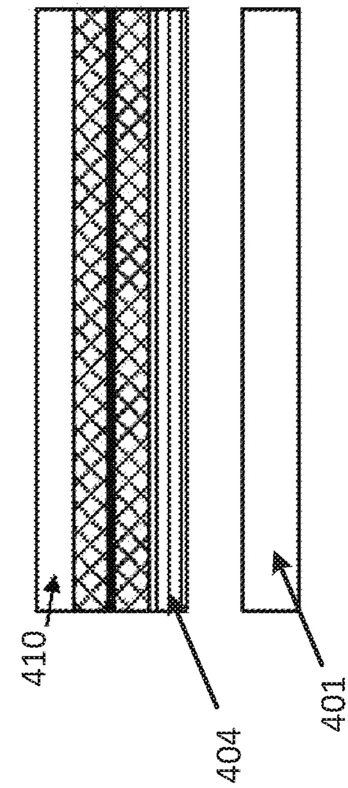


FIG. 13C

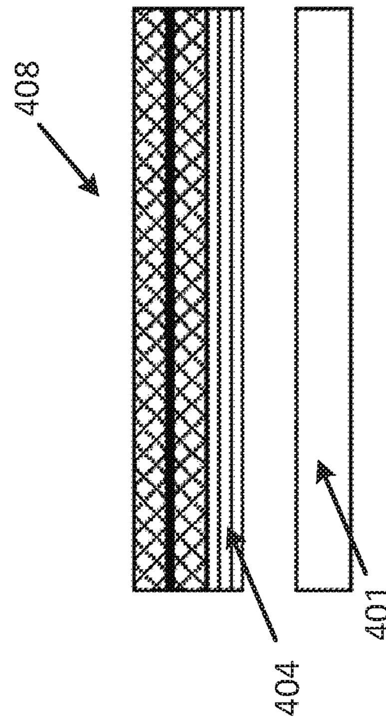


FIG. 13D

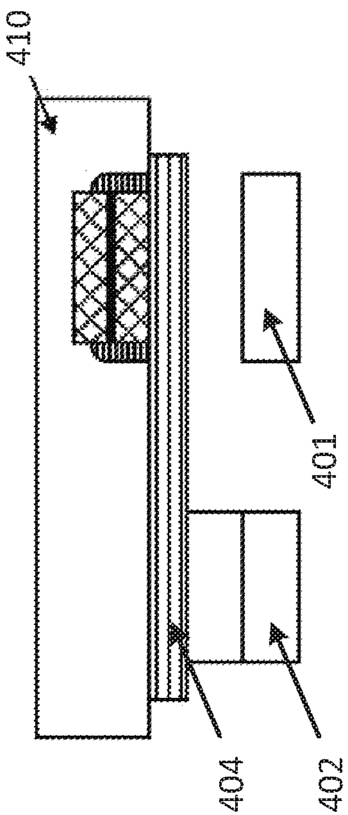


FIG. 12E

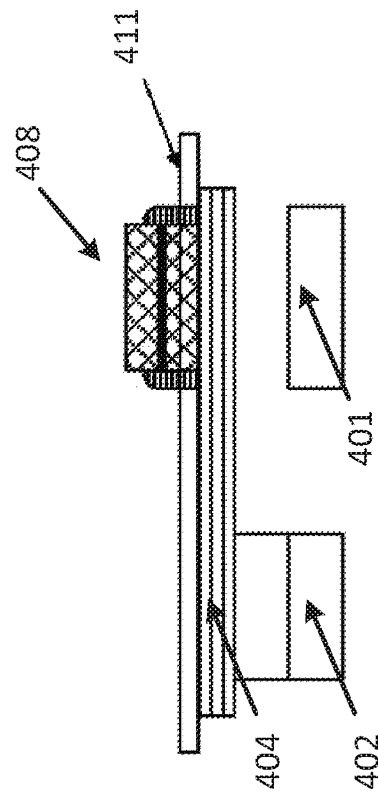


FIG. 12F

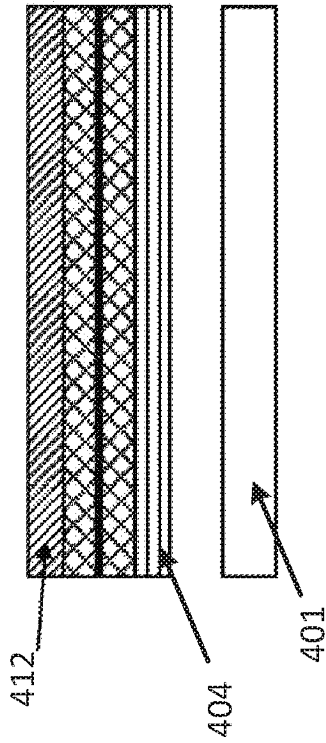


FIG. 13E

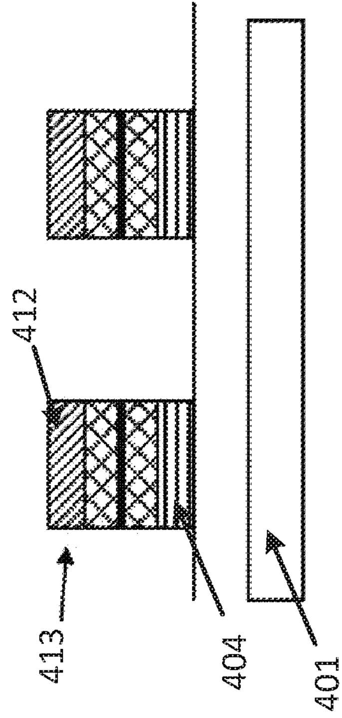


FIG. 13F

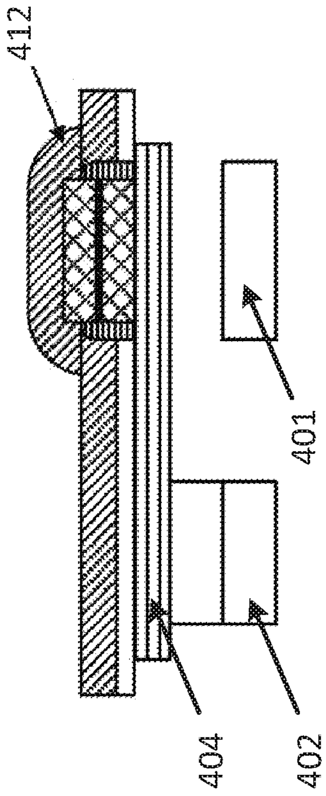


FIG. 12G

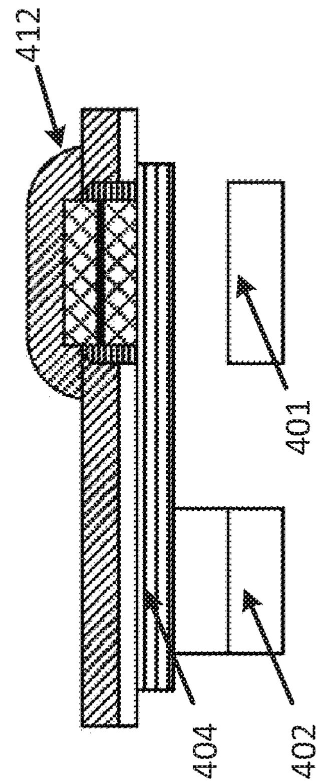


FIG. 12H

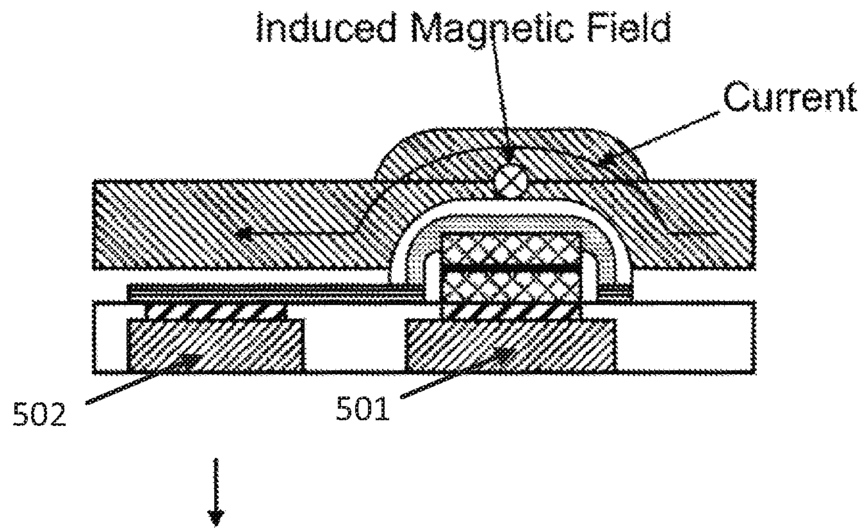


FIG. 14A

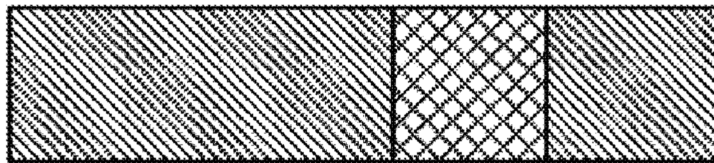


FIG. 14B

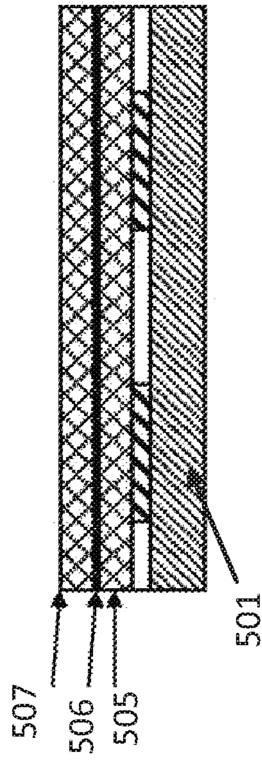


FIG. 16A

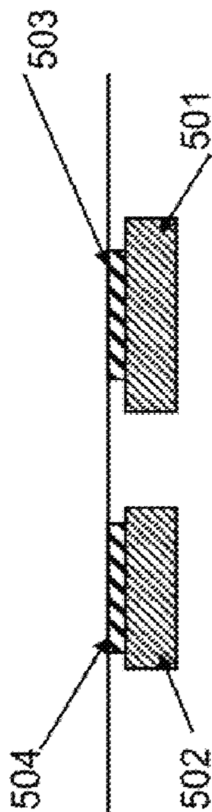


FIG. 15A

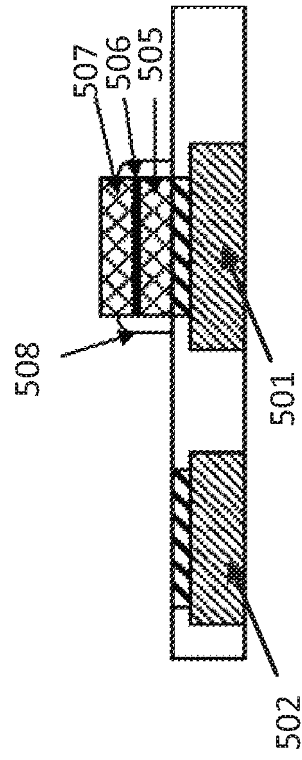


FIG. 15B

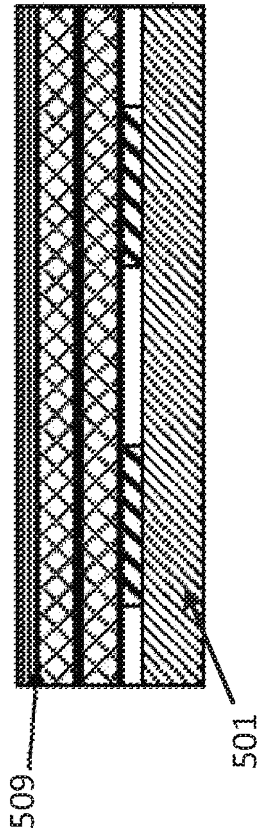


FIG. 16B

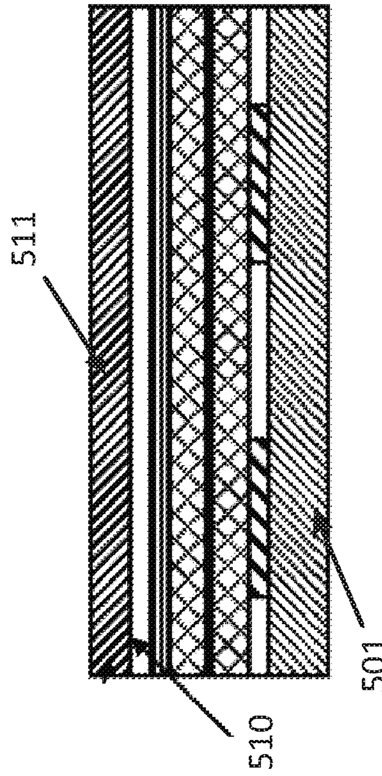


FIG. 16C

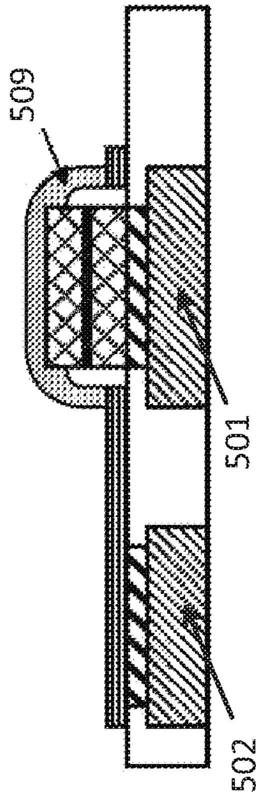


FIG. 15C

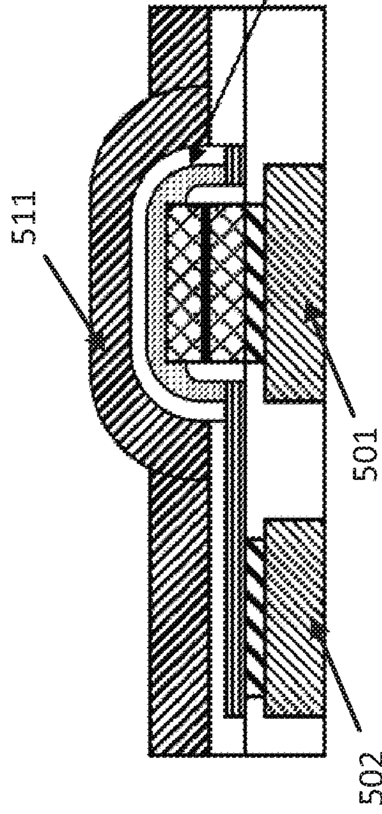


FIG. 15D

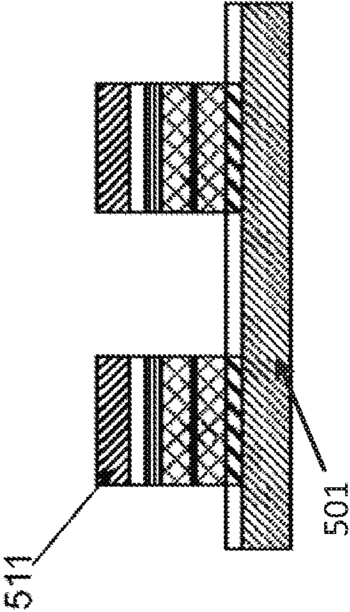


FIG. 16D

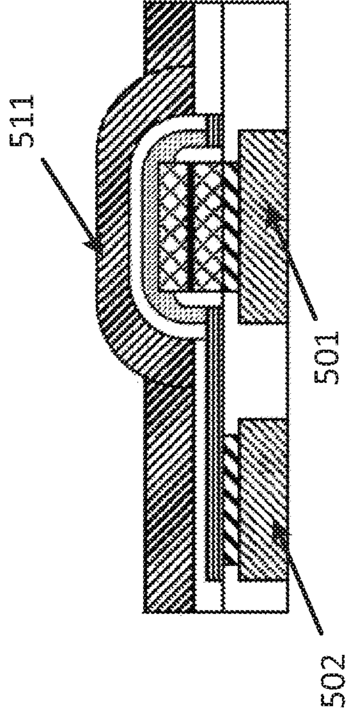


FIG. 15E

SELF CONTACTING BIT LINE TO MRAM CELL

[0001] This application is a continuation of U.S. patent application Ser. No. 14/886,370, titled "Self Contacting Bit Line to MRAM Cell," filed Oct. 19, 2015, which is a divisional of U.S. patent application Ser. No. 13/444,805, titled "Self Contacting Bit Line to MRAM Cell," filed Apr. 11, 2012, which claims the benefit of priority to U.S. Provisional Patent Application No. 61/473,921, titled "Self Contacting Bit Line to MRAM Cell," filed Apr. 11, 2011.

FIELD

[0002] Embodiments of the invention relate to MRAM (Magnetic Random Access Memory) semiconductor devices.

BACKGROUND

[0003] MRAM (Magnetic Random Access Memory) cells may be fabricated during BEOL (Back End Of Line) after a MOS FET device process. The minimum feature size of an MRAM cell is often 1.5× larger than that of FEOL (Front End of Line). It is therefore difficult to shrink memory size compared with other FEOL based memories.

SUMMARY

[0004] Embodiments of the invention disclose a plurality of self-aligned structures that save the overlay margin.

[0005] The first embodiment discloses a MTJ cell wherein the MTJ stack is directly coupled to the upper metal without the requirement of a via. Sidewalls of individual MTJ elements are protected with dielectric film spacer to prevent from PIN-Switch layer shorting **10** through the tunnel oxide layer. The top layer of MTJ is exposed to upper metal. Overlay margin in this embodiment is required only for upper metal coverage over MTJ. The upper metal width comes to f+2∂, saving 2∂ compared to previous art. Putting MTJ feature size equal to that of FEOL, the memory size becomes competitive to FEOL based memory.

[0006] The second embodiment comprises an electrically conductive material such as Titanium Nitride, which is used as a hard mask. The hard mask is for MTJ stack etch and remains on top of MTJ pillar after the etching. Inter layer oxide is deposited over the MTJ pillar. The hard mask remained on MTJ is exposed with CMP. Metal such as Al/Cu is deposited and patterned with conventional lithography and Reactive Ion Etching. The same reduction in memory cell size as the first embodiment is provided by the second embodiment.

[0007] The third embodiment discloses a self-aligned via which replaces the hard mask. Silicon nitride is used as hard mask as an example. The hard mask is for MTJ stack etch and remains on top of MTJ pillar after the etching. Inter layer oxide is deposited over the MTJ pillar. The hard mask remained on MTJ is exposed with CMP or Dual Damascene oxide trench etch. The exposed hard mask is removed by hot phosphoric acid followed by upper metal deposition. The same squeezing memory cell size as the first embodiment is expected on the structure.

[0008] The fourth embodiment is of self-aligned etching. MTJ is to be etched twice along word line direction first and bit line direction 2nd. Putting dielectric film, nitride preferred, spacer on MTJ pillar to prevent PIN layer—Fix layer short. Oxide is deposited and planerized by CMP. The oxide is recessed until MTJ appeared. Upper metal layer is deposited patterned. MTJ and bottom read lead is etched with the same mask as upper metal. The upper metal is wrapping around MTJ pillar. It works to help induce magnetic field. The upper metal width can be same size as MTJ pillar. It saves 4∂ compared with prior arts.

[0009] The fifth embodiment is also of self-aligned patterning. It is different in read electrode connecting to top of MTJ instead of bottom of the pillar. MTJ is connected to lower metal (write word line). Top metal is electrically isolated from MTJ with a thin dielectric film. The upper metal also wraps around MTJ. It enhances magnetic field induction for switching. It saves cell footprint also by 4∂.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] While the appended claims set forth the features of the present invention with particularity, the invention, together with its objects and advantages, will be more readily appreciated from the following detailed description, taken in conjunction with the accompanying drawings, wherein:

[0011] FIG. **1**A illustrates a cross-sectional view of prior arts.

[0012] FIG. **1**B illustrates a top view of prior arts.

[0013] FIG. **2**A illustrates a cross-sectional view of 1st preferred embodiment

[0014] FIG. **2**B illustrates a top view of 1st preferred embodiment.

[0015] FIG. **3**A to FIG. **3**H illustrate cross sectional views along bit line direction at individual process steps to the 1st embodiment

[0016] FIG. **4**A to FIG. **4**F illustrate cross sectional views along other direction of FIG. **3**C to FIG. **3**H.

[0017] FIG. **5**A illustrates a cross-sectional view of 2nd preferred embodiment.

[0018] FIG. **5**B illustrates a top view 2nd preferred embodiment.

[0019] FIG. **6**A to FIG. **6**F illustrate cross sectional views along bit line direction at individual process steps to the 2nd embodiment.

[0020] FIG. **7**A to FIG. **7**D illustrate cross sectional views along other direction of FIG. **6**C to FIG. **6**F.

[0021] FIG. **8**A illustrates a cross-sectional view of 3rd embodiment.

[0022] FIG. **8**B illustrates a top view 3rd embodiment.

[0023] FIG. **9**A to FIG. **9**H illustrate cross sectional views along bit line direction at individual process steps to the 3rd embodiment.

[0024] FIG. **10**A to FIG. **10**D illustrate cross sectional views along other direction of FIG. **9**E to FIG. **9**H.

[0025] FIG. **11**A illustrates a cross-sectional view of 4th embodiment.

[0026] FIG. **11**B illustrates a top view 4th embodiment.

[0027] FIG. **12**A to FIG. **12**H illustrate cross sectional views along bit line direction at individual process steps to the 4th embodiment.

[0028] FIG. **13**A to FIG. **13**F illustrate cross sectional views along other direction of FIG. **12**C to FIG. **12**H.

[0029] FIG. **14**A illustrates a cross-sectional view of 5th preferred embodiment.

[0030] FIG. **14**B illustrates a top view 5th embodiment.

[0031] FIG. **15**A to FIG. **15**E illustrate cross sectional views along bit line direction at individual process steps to the 5th embodiment.

[0032] FIG. **16**A to FIG. **16**D illustrate cross sectional views along other direction of FIG. **15**B to FIG. **15**E.

DETAILED DESCRIPTION

[0033] In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form only in order to avoid obscuring the invention.

[0034] Reference in this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearance of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment, nor are separate or alternative embodiments mutually exclusive of other embodiments. Moreover, various features are described which may be exhibited by some embodiments and not by others. Similarly, various requirements are described which may be requirements for some embodiments but not other embodiments.

[0035] Moreover, although the following description contains many specifics for the purposes of illustration, anyone skilled in the art will appreciate that many variations and/or alterations to said details are within the scope of the present invention. Similarly, although many of the features of the present invention are described in terms of each other, or in conjunction with each other, one skilled in the art will appreciate that many of these features can be provided independently of other features. Accordingly, this description of the invention is set forth without any loss of generality to, and without imposing limitations upon, the invention.

[0036] Prior Art FIG. **1**A shows a cross-sectional view through a prior art MRAM cell, whereas Prior Art FIG. **1**B shows a plan view of the MRAM cell. As can be seen the MRAM cell includes a MTJ (Magnetic Tunnel Junction) as a memory element. The MTJ is connected to upper and lower metals through via holes where overlay margin ∂ is required on the both edges of via hole landing area. The MTJ cell is designed to be bigger than the upper through hole to upper metal by 2∂. Since the upper metal should cover the MTJ, the upper metal becomes bigger than the MTJ by 2∂. The upper metal width consequently becomes 4∂ bigger than a feature size f of the via hole. Overlay margin is estimated to be 20% to 30% of the minimum feature size. The metal width would be twice bigger than minimum feature size.

[0037] FIG. **2**A shows a cross sectional view of a first embodiment of an MRAM cell. A top view of the first embodiment is shown in FIG. **2**C. As will be seen, the upper metal **113** is directly connected to the top of MTJ. Overlay margin of MTJ to via is not necessary so that upper metal width becomes $f+2\partial$ considering overlay margin of upper metal to MTJ. Thus, the first embodiments saves 2∂ compared to conventional structure showed in Prior Art FIG. **1**A and Prior Art FIG. **1**B.

[0038] As shown in FIG. **3**A, a lower metal as write word line **101** and landing pad **102** to read device are patterned after the FEOL process is completed. The surface over write word line is planerized with CMP. Bottom read lead **104**, MTJ Pin layer **105**, tunnel oxide **106**, MTJ fixed layer **107** and hard mask layer are subsequently deposited as shown in FIG. **3**B. Patterning photo resist **108** with MTJ pillar mask in FIGS. **3**C and **4**A, MTJ stack (**107**, **106**, **105**) is etched with ion milling or reactive ion etch with end point at read lead metal **104** surface. Read lead metal is patterned with photo resist mask **109** and etched also with ion milling or reactive ion etch as shown in FIGS. **3**D and **4**B. A dielectric layer having enough etch selectivity to oxide such as nitride is deposited and vertically etched as shown in FIGS. **3**E and **4**C to put dielectric spacer **110** on MTJ sidewall to protect the junction **106**. Oxide **111** as an inter dielectric layer is deposited and planerized as shown in FIGS. **3**F and **4**D. Trench line **112** is formed in oxide **111** using conventional damascene process. The trench etch goes until top of MTJ surface completely appears as shown in FIGS. **3**G and **4**E. Seed layer is deposited and copper **112** is plugged in trench with electro plating. Conventional copper CMP is used to remove excess copper outside of the trench as shown in FIGS. **3**H and **4**F.

[0039] A cross sectional view of the 2nd embodiment is shown in FIG. **5**A. Top view is in FIG. **5**B. The MTJ pillar is coupled to the upper metal **213** without the need of a via. Overlay margin of MTJ to via is thus not necessary so that upper metal width becomes $f+2\partial$ considering overlay margin of upper metal to MTJ as discussed in the first embodiment. This embodiment saves 2∂ compared to conventional structure shown in Prior Art FIG. **1**A and FIG. **1**B.

[0040] As shown in FIG. **6**A, lower metal as write word line **201** and landing pad **202** to read device are patterned after FEOL process is completed. The surface over write word line is planerized with CMP. Bottom read lead **204**, MTJ Pin layer **205**, tunnel oxide **206**, MTJ fixed layer **207** and hard mask layer **208** consisting of oxide and Titanium nitride are subsequently deposited as shown in FIG. **6**B. Titanium Nitride layer and oxide layer **208** are patterned using conventional lithography and mask etch as shown in FIGS. **6**C and **7**A. Vertical ion etching with Ion milling or reactive ion allows to transfer the hard mask pattern into MTJ stack as in FIGS. **6**D and **7**B, with end point at read lead metal **204** surface, followed by read lead metal patterning similar to the first embodiment. Oxide **210** as an inter dielectric layer is deposited as shown in FIGS. **6**E and **7**C. CMP is allowed until Titanium nitride appears on surface as shown in FIGS. **6**F and **7**D, followed by conventional metal dry etch process.

[0041] A cross-sectional view of the 3rd embodiment is shown in FIG. **8**A. A top view of the 3rd embodiment is shown in FIG. **8**B. A self-aligned via connects the MTJ pillar/stack to the upper metal. Overlay margin of MTJ to via is not necessary so that upper metal width becomes $f+2\partial$ considering overlay margin of upper metal to MTJ as discussed in the first embodiment. It save 2∂ compared to conventional structure showed in Prior Art FIG. **1**A. and FIG. **1**B.

[0042] As shown in FIG. **9**A, lower metal as write word line **301** and landing pad **302** to read device are patterned after FEOL process is completed. The surface over write word line is planerized with CMP. Bottom read lead **304**, MTJ Pin layer **305**, tunnel oxide **306**, MTJ fixed layer **307** and hard mask layer consisting of bottom oxide **308** and nitride **309** are subsequently deposited as shown in FIG. **9**B.

Nitride layer and oxide layer are patterned using conventional lithography and mask etch as shown in FIG. **9**C. Vertical ion etching with Ion milling or reactive ion etch allows to transfer the hard mask pattern into MTJ stack as in FIG. **9**D, with end point at read lead metal **304** surface, followed by read lead metal patterning similar to the first embodiment. Oxide **310** as an inter dielectric layer is deposited and planerized as shown in FIGS. **9**E and **10**A. Trench line **311** is formed in oxide **310** using conventional damascene process. The trench etch goes until top of hard mask nitride surface completely appears as shown in FIGS. **9**F and **10**B. Exposed nitride **309** is removed with hot phosphoric acid as shown in FIGS. **9**G and **10**C. The self aligned via structure **312** delivered. Adding oxide etch, the oxide **308** over MTJ is etched and MTJ surface appears. Seed layer is deposited and copper **313** is plugged in trench with electro plating. Conventional copper CMP remove excess copper outside of the trench as shown in FIGS. **9**H and **10**D.

[0043] A cross-sectional view of the 4th embodiment is shown in FIG. **11**A. A top view of the 4th embodiment is shown in FIG. **11**B. MTJ is patterned twice. Firstly along the word line direction and secondly along the bit line direction. At 2nd patterning, upper metal layer, MTJ and bottom read lead are patterned with one mask. No overlay margin is required so that upper metal width becomes same feature size as MTJ. This embodiment saves 4∂ compared to conventional structure showed in Prior Art FIG. **1**A and FIG. **1**B. The structure has other benefit than cell size. The upper metal wraps around the MTJ. The current flowing the metal induces stronger magnetic field than straight metal line. It works better to switch the pin layer direction.

[0044] As shown in FIG. **12**A, lower metal as write word line **401** and landing pad **402** to read device are patterned after FEOL process is completed. The surface over write word line is planerized with CMP. Bottom read lead **404**, MTJ Pin layer **405**, tunnel oxide **406**, MTJ fixed layer **407** and hard mask layer are subsequently deposited as shown in FIG. **12**B. With the same process step as previous embodiments, MTJ stack **408** is patterned as a line along word line direction as shown in FIG. **12**C and FIG. **13**A. Nitride spacer **409** is placed on side wall of MTJ line as shown in FIGS. **12**D and **13**B. Oxide **410** is deposited and planerized as shown in FIGS. **12**E and **13**C. The planerized oxide is recessed with vertical ion etching until top of MTJ line appears enough as shown in FIGS. **12**F and **13**D. Remained oxide **411** in FIG. **12**F is to insulate upper metal from bottom read lead metal. Upper metal **412** such as aluminum/Cu alloy is deposited as shown in FIGS. **12**G and **13**E. Patterning photoresist, the upper metal is etched with conventional metal etching process by reaching to insulation oxide **411**. Subsequent Ion milling etches oxide, MTJ and bottom read lead metal to get self-aligned structure **413** as shown in FIGS. **12**H and **13**F.

[0045] A cross-sectional view of the 5th embodiment is shown in FIG. **14**A. A top view of the 5th embodiment is shown in FIG. **14**B. MTJ is connected lower metal line (write word line) instead of connecting upper metal as adapted in previous embodiments. Read lead is connected to top of MTJ different from previous 4 embodiments. Thin oxide separates upper metal and read lead/MTJ electrically. MTJ is also patterned twice along word line direction first and bit line direction 2nd as was the case with the 4th embodiment. At 2nd patterning, upper metal layer, MTJ and bottom read lead are patterned with one mask. No overlay margin is required so that upper metal width becomes same feature size as MTJ. It save 4∂ compared to conventional structure showed in Prior Art FIG. **1**A and FIG. **2**B. The structure has other benefit than cell size. The upper metal wraps around the MTJ. The current flowing the metal induces stronger magnetic field than straight metal line. It works better to switch the pin layer direction.

[0046] As shown in FIG. **15**A, lower metal as write word line **501** and landing pad **502** to read device are patterned after FEOL process is completed. The vias **503** and **504** to be connected to MTJ and read lead metal are opened over **501** and **502**.

[0047] Tungsten is deposited and allows CMP to make the surface smooth. MTJ Pin layer **505**, tunnel oxide **506**, MTJ fixed layer **507** and hard mask layer are subsequently deposited as previous embodiments. The stack is patterned as a line along the word line direction and followed by spacer oxide protect the MTJ sidewall as shown in FIGS. **15**B and **16**A. Read metal **509** is deposited and patterned as shown in FIGS. **15**C and **16**B. With the same process step as previous embodiments, Thin oxide **510** is deposited to insulate MTJ/Read Metal and upper metal(Bit line). Upper metal **511** such as aluminum/Cu alloy is deposited as shown in FIGS. **15**D and **16**C. Patterning photoresist, the upper metal is etched with conventional metal etching process by reaching to insulation oxide **510**. Oxide **510** can be removed by wet etch. Subsequent Ion milling etches read lead metal, MTJ as shown in FIGS. **15**E and **16**D.

[0048] Although the present invention has been described with reference to specific exemplary embodiments, it will be evident that the various modification and changes can be made to these embodiments without departing from the broader spirit of the invention. Accordingly, the specification and drawings are to be regarded in an illustrative sense rather than in a restrictive sense.

1-18. (canceled)

19. A method of fabricating a magnetic memory cell, the method comprising:

forming a write word line and a landing pad in a substrate such that an upper surface of the write word line is below an upper surface of the substrate;

forming a read lead layer on the upper surface of the substrate and electrically coupled to the landing pad;

forming a plurality of memory element layers such that at least one memory element layer is electrically coupled to the read lead layer;

forming a hard mask layer over the plurality of memory element layers;

patterning the hard mask layer to form a hard mask pattern comprising a hard mask cap positioned over the write word line;

transferring the hard mask pattern to the plurality of memory element layers to form a memory element stack from the plurality of memory element layers, wherein the memory element stack is positioned over the write word line and covered with the hard mask cap of the hard mask layer, and wherein the hard mask cap is self-aligned with the memory element stack as a result of said transferring the hard mask pattern;

depositing an oxide layer over the hard mask cap and the memory element stack;

forming a trench above the hard mask cap and the memory element stack by etching the oxide layer until at least a top surface of the hard mask cap is exposed;

removing the hard mask cap exposed via the trench to obtain a hole that is self-aligned with the memory element stack;

depositing a seed layer in the hole; and

filling the hole and the trench with conductive material to obtain a conductive structure that is self-aligned with the memory element stack.

20. The method of claim **19**, wherein said forming the plurality of memory element layers comprises:

forming a pin layer;

forming a tunnel oxide layer on the pin layer; and

forming a fixed layer on the tunnel oxide layer.

21. The method of claim **20**, wherein said transferring the hard mask pattern comprises transferring the hard mask pattern to the fixed layer, the tunnel oxide layer, and the pin layer to obtain the memory element stack.

22. The method of claim **19**, wherein:

said patterning the hard mask layer comprises performing a lithographic and mask etch process to form the hard mask pattern from the hard mask layer; and

said transferring the hard mask pattern to the plurality of memory element layers comprises, after the lithographic and mask etch process, ion milling the plurality of memory element layers using the hard mask cap of the hard mask pattern as a mask to form the memory element stack, wherein said ion milling self-aligns the hard mask cap with the memory element stack.

23. The method of claim **19**, wherein said filling the hole and trench forms another read lead layer that is electrically coupled to the memory element stack.

24. The method of claim **19**, wherein the hard mask layer comprises an oxide layer formed over the plurality of memory element layers and a nitride layer formed over the oxide layer of the hard mask layer.

25. The method of claim **24**, wherein said removing the hard mask cap comprises:

using an acid to remove the nitride layer of the hard mask cap; and

etching the oxide layer of the hard mask cap until at least an upper surface of the memory element stack is exposed.

26. The method of claim **25**, wherein said filling the hole and the trench comprises plugging copper in the trench with electroplating.

27. The method of claim **25**, further comprising removing excess copper outside of the trench via chemical mechanical polishing.

28. The method of claim **19**, wherein:

said patterning the hard mask layer comprises performing a lithographic and mask etch process to form the hard mask pattern from the hard mask layer; and

said transferring the hard mask pattern to the plurality of memory element layers comprises, after the lithographic and mask etch process, reactive ion etching the plurality of memory element layers using the hard mask cap of the hard mask pattern as a mask to form the memory element stack, wherein said reactive ion etching self-aligns the hard mask cap with the memory element stack.

29. A method of fabricating a magnetic memory cell, the method comprising:

forming a write word line and a landing pad in a substrate such that an upper surface of the write word line is below an upper surface of the substrate;

forming a read lead layer on the upper surface of the substrate and electrically coupled to the landing pad;

forming a plurality of memory element layers such that at least one memory element layer is electrically coupled to the read lead layer;

forming a hard mask layer over the plurality of memory element layers;

patterning the hard mask layer to form a hard mask pattern comprising a hard mask cap positioned over the write word line;

transferring the hard mask pattern to the plurality of memory element layers to form a memory element stack from the plurality of memory element layers, wherein the memory element stack is positioned over the write word line and covered with the hard mask cap of the hard mask layer, and wherein the hard mask cap is self-aligned with the memory element stack as a result of said transferring the hard mask pattern;

depositing an oxide layer over the hard mask cap and the memory element stack;

forming a trench above the hard mask cap and the memory element stack by etching the oxide layer until at least a top surface of the hard mask cap is exposed;

removing the hard mask cap exposed via the trench to obtain a hole that is self-aligned with the memory element stack; and

electroplating the trench and the hole with copper.

30. The method of claim **29**, wherein said forming the plurality of memory element layers comprises:

forming a pin layer;

forming a tunnel oxide layer on the pin layer; and

forming a fixed layer on the tunnel oxide layer.

31. The method of claim **30**, wherein said transferring the hard mask pattern comprises transferring the hard mask pattern to the fixed layer, the tunnel oxide layer, and the pin layer to obtain the memory element stack.

32. The method of claim **29**, wherein:

said patterning the hard mask layer comprises performing a lithographic and mask etch process to form the hard mask pattern from the hard mask layer; and

said transferring the hard mask pattern to the plurality of memory element layers comprises, after the lithographic and mask etch process, ion milling the plurality of memory element layers using the hard mask cap of the hard mask pattern as a mask to form the memory element stack, wherein said ion milling self-aligns the hard mask cap with the memory element stack.

33. The method of claim **29**, wherein said electroplating forms another read lead layer that is electrically coupled to the memory element stack.

34. The method of claim **29**, wherein the hard mask layer comprises an oxide layer formed over the plurality of memory element layers and a nitride layer formed over the oxide layer of the hard mask layer.

35. The method of claim **34**, wherein said removing the hard mask cap comprises:

using an acid to remove the nitride layer of the hard mask cap; and

etching the oxide layer of the hard mask cap until at least an upper surface of the memory element stack is exposed.

36. The method of claim **29**, wherein:

said patterning the hard mask layer comprises performing a lithographic and mask etch process to form the hard mask pattern from the hard mask layer; and

said transferring the hard mask pattern to the plurality of memory element layers comprises, after the lithographic and mask etch process, reactive ion etching the plurality of memory element layers using the hard mask cap of the hard mask pattern as a mask to form the memory element stack, wherein said reactive ion etching self-aligns the hard mask cap with the memory element stack.

37. A method of fabricating a magnetic memory cell, the method comprising:

forming a write word line and a landing pad in a substrate such that an upper surface of the write word line is below an upper surface of the substrate;

forming a read lead layer on the upper surface of the substrate and electrically coupled to the landing pad;

forming a plurality of memory element layers such that at least one memory element layer is electrically coupled to the read lead layer;

transferring a pattern of a hard mask layer to the plurality of memory element layers to form a memory element stack from the plurality of memory element layers, wherein the memory element stack is positioned over the write word line and covered with a hard mask cap of the hard mask layer;

after said transferring of the hard mask pattern to the plurality of memory element layers, etching the read lead layer to form a plurality of read leads that include a read lead electrically coupled to the memory element stack;

depositing an oxide layer over the hard mask cap and the memory element stack;

etching a trench into the oxide layer until at least a top surface of the hard mask cap is exposed;

removing the hard mask cap exposed via the trench to obtain a hole aligned with the memory element stack; and

filling the hole and the trench with conductive material to obtain a conductive structure that is aligned with the memory element stack.

38. The method of claim **37**, wherein said filling the hole and trench forms another read lead layer that is electrically coupled to the memory element stack.

* * * * *