OP \$165,00 36174

TRADEMARK ASSIGNMENT

Electronic Version v1.1 Stylesheet Version v1.1

SUBMISSION TYPE: NEW ASSIGNMENT

NATURE OF CONVEYANCE: Security Agreement

CONVEYING PARTY DATA

Name	Name Formerly		Entity Type
CALIFORNIA MICRO DEVICES CORPORATION		02/25/2010	CORPORATION: DELAWARE

RECEIVING PARTY DATA

Name:	JPMORGAN CHASE BANK, N.A., as collateral agent
Street Address:	270 Park Avenue
City:	New York
State/Country:	NEW YORK
Postal Code:	10017
Entity Type:	Association: UNITED STATES

PROPERTY NUMBERS Total: 6

Property Type	Number	Word Mark	
Registration Number:	3617486	C.MD	
Registration Number:	3548014	PICOGUARD	
Registration Number:	3136826	PRAETORIAN	
Registration Number:	3555054	XTREMEESD	
Registration Number:	3741111	LUXGUARD	
Serial Number:	77695150	LUXGUARD	

CORRESPONDENCE DATA

Fax Number: (866)826-5420

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: 3016380511

Email: ipresearchplus@comcast.net

Correspondent Name: IP Research Plus, Inc. Address Line 1: 21 Tadcaster Circle

Address Line 2: Attn: Penelope J.A. Agodoa

Address Line 4: Waldorf, MARYLAND 20602

900157080 REEL: 004167 FRAME: 0287

TRADEMARK

ATTORNEY DOCKET NUMBER:	35497
NAME OF SUBMITTER:	Penelope J.A. Agodoa
Signature:	/pja/
Date:	03/15/2010
Total Attachments: 9 source=35497#page1.tif source=35497#page2.tif source=35497#page3.tif source=35497#page4.tif source=35497#page5.tif source=35497#page6.tif source=35497#page7.tif source=35497#page8.tif source=35497#page8.tif	

RECORDATION FORM COVER SHEET TRADEMARKS ONLY				
To the Director of the U. S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.				
Name of conveying party(ies): CALIFORNIA MICRO DEVICES CORPORATION	2. Name and address of receiving party(ies) Additional names, addresses, or citizenship attached? ✓ No			
☐ Individual(s) ☐ Association ☐ General Partnership ☐ Limited Partnership ☑ Corporation- State: DELAWARE ☐ Other ☐ Citizenship (see guidelines) ☐ Additional names of conveying parties attached? ☐ Yes ☐ No 3. Nature of conveyance)/Execution Date(s): Execution Date(s) 2/25/2010 ☐ Assignment ☐ Merger ☑ Security Agreement ☐ Change of Name	General Partnership Citizenship Limited Partnership Citizenship Corporation Citizenship Other Citizenship If assignee is not domiciled in the United States, a domestic representative designation is attached: Yes No			
4. Application number(s) or registration number(s) and identification or description of the Trademark. A. Trademark Application No.(s) PLEASE SEE SCHEDULE ATTACHED B. Trademark Registration No.(s) PLEASE SEE SCHEDULE ATTACHED Additional sheet(s) attached? Yes C. Identification or Description of Trademark(s) (and Filing Date if Application or Registration Number is unknown)				
5. Name & address of party to whom correspondence concerning document should be mailed: Name: IP Research Plus	6. Total number of applications and registrations involved:			
Internal Address: Attn: Penelope J.A. Agodoa Street Address:21 Tadcaster Circle	7. Total fee (37 CFR 2.6(b)(6) & 3.41) \$ Authorized to be charged by credit card Authorized to be charged to deposit account Enclosed			
City: Waldorf State: MD Zip: 20602	8. Payment Information: a. Credit Card Last 4 Numbers Expiration Date			
Phone Number: 301-638-0511 Fax Number: 866-826-5420 Email Address: orders@ipresearchplus.com	b. Deposit Account Number Authorized User Name			
9. Signature: Michael Charles Signature	3/2/2010 Date Total number of pages including cover			
Jordana Dreyfuss Name of Person Signing	sheet, attachments, and document:			

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to: Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450

PATENT SECURITY AGREEMENT, dated as of February 25, 2010, between CALIFORNIA MICRO DEVICES CORPORATION, a Delaware corporation and JPMORGAN CHASE BANK, N.A., a national banking association as collateral agent (the "Collateral Agent").

Reference is made to the Security Agreement dated as of August 4, 1999, as amended and restated as of March 3, 2003 (as amended, supplemented or otherwise modified from time to time, the "Security Agreement"), among Semiconductor Components Industries, LLC, a Delaware limited liability company, ON Semiconductor Corporation, a Delaware corporation, the Subsidiary Loan Parties and the Collateral Agent. The Lenders have agreed to extend credit to the Borrower subject to the terms and conditions set forth in the Credit Agreement dated as of August 4, 1999, as amended and restated as of March 6, 2007 (as amended, supplemented or otherwise modified from time to time (the "Credit Agreement")). The obligations of the Lenders to continue to extend such credit are conditioned upon, among other things, the execution and delivery of this Patent Security Agreement (this "Agreement"). Accordingly, the parties hereto agree as follows:

SECTION 1. <u>Terms.</u> Capitalized terms used in this Agreement and not otherwise defined herein have the meanings specified in the Security Agreement. The rules of construction specified in Section 1.03 of the Security Agreement also apply to this Agreement.

SECTION 2. <u>Grant of Security Interest.</u> As security for the payment or performance, as the case may be, in full of the Obligations, each Grantor, pursuant to the Security Agreement, did and hereby does grant to the Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest in, all right, title or interest in or to any and all of the following assets and properties now owned or at any time hereafter acquired by such Grantor or in which such Grantor now has or at any time in the future may acquire any right, title or interest (collectively, the "<u>Patent Collateral</u>"):

(a) all letters patent of the United States or any other country, all registrations and recordings thereof, and all applications for letters patent of the United States or any other country, including registrations, recordings and pending applications in the United States Patent and Trademark Office or any similar offices in any other country, including those listed on Schedule 1 (the "Patents"), and all reissues, continuations, divisions, continuations-in-part, renewals or extensions thereof, and the inventions disclosed or claimed therein, including the right to make, use and/or sell the inventions disclosed or claimed therein.

SECTION 3. <u>Termination</u>. This Agreement is made to secure the satisfactory performance and payment of the Obligations. Upon termination of the Security Agreement or release of a Grantor's obligations thereunder, this Agreement shall automatically terminate as to such Grantor.

[[NYCORP:3199335]]

SECTION 4. <u>Security Agreement</u>. The security interests granted to the Collateral Agent herein are granted in furtherance, and not in limitation of, the security interests granted to the Collateral Agent pursuant to the Security Agreement. Each Grantor hereby acknowledges and affirms that the rights and remedies of the Collateral Agent with respect to the Patent Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are hereby incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Agreement and the Security Agreement, the terms of the Security Agreement shall govern.

[[NYCORP:3199335]]

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

CALIFORNIA MICRO DEVICES					
CORPORATION)					
by					
Name: Donald A. Colvin					
Title: Director & Treasurer					
IDMOD CAN CHACE DANK AND					

JPMORGAN CHASE BANK, N.A., as Collateral Agent,

by				
-	Name:	 	 	
	Title:			

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

CALIFORNIA MICRO DEVICES CORPORATION

ру		
40	Name:	-
	Title:	
	RGAN CHASE BANK, N.A., as	
Collate	ral Agent,	

by

Name:

Title:

Ann B. Kerns Vice President

SCHEDULE 1

Patents and Trademarks

I. Registered U.S. Trademarks.

Mark	Registration No.	Registration Date
C.MD DESIGN	3617486	05-05-2009
PICOGUARD	3548014	12-16-2008
PRAETORIAN	3136826	08-29-2006
XTREMEESD	3555054	12-30-2008
LUXGUARD	3741111	01-19-2010

II. <u>U.S. Trademarks Applied For and Registration Pending.</u>

	Description	Application No.	Filing Date
,	LUXGUARD	77/695150	03-19-2009

III. <u>Trademark Licenses</u>. See <u>Annex 1</u> attached hereto.

IV. Registered U.S. Patents.

Description	Patent No.	Issue Date
Silicon Sub Mount Capable of Single Wire Bonding and of Providing ESD Protection for Light Emitting Diode Devices	6642550	11/4/2003
ESD Protected Thin Film Capacitor Structures	6121669	9/19/2000
ESD Protected Thin Film Capacitor Structures	5706163	1/6/1998
Integrated Resistor Networks Having Reduced Cross Talk	5652460	7/29/1997
Methods and Apparatus for Improving Frequency Response of Integrated RC Filters with Additional Ground Pins	5760662	6/2/1998
Integrated Circuit Structures and Methods to Facilitate Accurate Measurement of the IC Devices	6262434	7/17/2001
Method for Programmable Integrated Passive Devices	5998275 (reissued)	12/7/1999
Programmable Integrated Passive Devices	6281564 And RE38550	8/28/2001 7/6/2004
Termination Circuits and Methods for Bused and Networked Devices	6307395	10/23/2001
Termination Circuits and Methods for Memory Buses and Devices	6100713	8/8/2000
Termination Circuits and Methods therefore	6326805	12/4/2001
Termination Circuits and Methods therefore	6331787	12/18/2001

٠	Termination Circuits and Methods therefore	6329837	12/11/2001
ι	Termination Circuits and Methods therefore	6331786	12/18/2001
15	Termination Circuits and Methods therefore	6323676	11/27/2001
	Termination Circuits and Methods therefore	6326804	12/4/2001
	Termination Circuits and Methods therefore	6323675	11/27/2001
	Low Drop Out Regulator Capable of Functioning in Linear and Saturated Regions of Output Driver	6285246	9/4/2001
20	Voltage Trimmable Resistor	6452478	9/17/2002
•	Input Stage for Rail to Rail Input Amp	6031423	2/29/2000
•	Voltage Source Switching Circuit at Reduced Voltage Drop Levels	6285091	9/4/2001
	Integrated Electrical Overload Protection Device and Method of Formation	6201679	3/13/2001
4	Method and Apparatus for Non Linear Termination of a Transmission Line	6512393	1/28/2003
	Method and Apparatus for Non Linear Termination of a Transmission Line	6556040	4/29/2003
	Termination Circuits and Methods Therefor	6008665	12/28/1999
,	Method and Apparatus for Non Linear Termination of a Transmission Line	6747476	6/8/2004
	Method of Making a Semiconductor Device with Integrated RC Network and Schottky Diode	5514612	5/7/1996
9	Method of Making a Semiconductor Device with Integrated RC Network and Schottky Diode	5355014	10/11/1994
-	Methods for Fabrication of Thin Film Inductors, Inductor Networks, Inductor/Capacitor Filters, and Integration with Other Passive and Active Devices and the Resultant Devices	5788854	8/4/1998
	Methods for Fabrication of Thin Film Inductors, Inductor Networks and Integration with Other Passive and Active Devices	5370766	12/6/1994
	Semiconductor Device with Integrated RC Network and Schottky Diode	5770886	6/23/1998
.	BICMOS Track and Hold Amplifier	5291074	3/1/1994
,	Thin Film Inductors, Inductor Network and Integration with Other Passive and Active Devices	5450263	9/12/1995
	Method and Apparatus for Dynamic Impact Testing	7412870	8/19/2008
	System and Method for Startup Bootstrap for Internal Regulators	7002387	2/21/2006
ı	Apparatus and Method that Provides Active Pull Up and Logic Translation from one Signal Mode to Another Signal Mode	7446565	11/4/2008
.	Bidirectional Buffer with Slew Rate Control and Method of Bidirectionally Transmitting Signals with Slew Rate control	7321241	1/22/2008
	Method and Apparatus that Provides Differential Connections with Improved ESD Protection and Routing	7479680	1/20/2009
	Regulator for DDR DRAM Termination Voltage	6707280	3/16/2004
L	Wire Bond and Redistribution Layer Process	7541251	6/2/2009
	Low Operating voltage Electrostatic Discharge Device and Method	75 7 6370	8/18/2009
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Dual-Output Voltage Regulator	7057310	6/6/2006		

V. <u>U.S. Patents Applied For and Registration Pending.</u>

44

Description	Application No.	Filing Date
Integrated Passive Filter Incorporating Inductors and ESD Protectors	11/206,667	8/17/2005
Low Capacitance Solder bump Interface Structure	11/371,175	3/8/2006
Wire Bond and Redistribution Layer Process	12/476,847	6/2/2009
Slaving Video Presentation	11/566,022	12/1/2006
High Density Inductor	11/564,241	11/28/06
A High Current Steering ESD Protection Zener Diode and Method	11/738,176	4/20/07
Method of Making Reliable Wafer Level Chip Scale Packaging Semiconductor Devices	11/685,085	3/12/07
Method and Apparatus for Providing 2-Stage ESD Protection for High Speed Interfaces	12/180,440	7/25/08
Low Pass Filter Incorporating Coupled Inductors to Enhance Stop Band Attenuation	12/014,725	1/15/08
Impedance Compensated ESD Circuit for Protection for High-Speed Interfaces and Method of Using the Same	12/332,159	12/10/2008
Method of ESD Structure Layout Using Circular Patterns	12/434805	5/12/2009

VI. <u>Patent Licenses</u>. See <u>Annex 1</u> attached hereto.

VII. Registered U.S. Mask Work.

Title	Registration No.	Registration Date
CSPEMI1306	MW00000169 0 4	05-20-2003

ANNEX 1 TO SCHEDULE 1

Intellectual Property License Agreements

- 1. Arasan Chip Systems License Agreement between the New Grantor and Arasan Chip Systems, Inc., dated August 29, 2007. [Copyright]
- License Agreement between the New Grantor and Mixel, Inc., dated April 22, 2009.
 [Patent and Copyright]
- License Agreement between the New Grantor and True Circuits, Inc., dated August 15, 2007. [Patent and Copyright].
- 4. Development, Technical Support and Limited Use Agreement between the New Grantor and QUALCOMM Incorporated, dated April 29, 2009. [Copyright]
- 5. UMC FDK License Agreement between the New Grantor and United Microelectronics Corporation, dated June 29, 2009. [Patent and Copyright]
- 6. Development, Technical Support and Limited Use Agreement between the New Grantor and QUALCOMM Incorporated, dated December 17, 2004. [Patent and Copyright]
- 7. Specific Purpose License Agreement between the New Grantor and Cadence Design Systems, Inc., dated August 12, 2009. [Patent and Copyright]
- 8. End User Software License and Maintenance Agreement between the New Grantor and Synopsys, Inc., dated August 26, 2004. [Patent and Copyright]
- 9. Restricted Use License Agreement between the New Grantor and Intel Corporation, dated February 6, 1998.
- 10. Private Label Agreement between the New Grantor and Littelfuse, Inc., dated March 28, 2001. [Trademark]
- Oracle License and Services Agreement between the New Grantor and Oracle Corporation, dated May 31, 2004, as amended by the Amendment One, dated May 31, 2004. [Patent and Copyright]
- 12. Settlement Agreement between the New Grantor and Advanced Micro Devices, Inc., dated November 21, 2008. [Trademark]
- 14. Reseller Agreement between the New Grantor and GDA Technologies, Inc., dated September 11, 2009. [Patent]

TRADEMARK REEL: 004167 FRAME: 0297

RECORDED: 03/15/2010