

TRADEMARK ASSIGNMENT

Electronic Version v1.1
 Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE BY SECURED PARTY

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
FOCUS VENTURES II, LP		09/04/2009	LIMITED PARTNERSHIP: UNITED STATES

RECEIVING PARTY DATA

Name:	SEQUENCE DESIGN, INC.
Street Address:	440 North Wolfe Road
City:	Sunnyvale
State/Country:	CALIFORNIA
Postal Code:	94085
Entity Type:	CORPORATION: CALIFORNIA

PROPERTY NUMBERS Total: 21

Property Type	Number	Word Mark
Registration Number:	2162591	COLUMBUS
Registration Number:	2744939	POWERTHEATER
Registration Number:	2947349	ELMO
Registration Number:	2881000	COOLTIME
Registration Number:	2912433	SHOWTIME
Registration Number:	2912434	PHYSICALSTUDIO
Registration Number:	3003308	EXTRACTIONSTAGE
Registration Number:	3225732	COOLPOWER
Registration Number:	2252594	WATTWATCHER
Serial Number:	78590841	COOLTHEATRE
Serial Number:	78590851	COOL BY DESIGN
Serial Number:	78822255	COOLCHECK
Serial Number:	78727932	NANOCOOL

CH \$540.00 2162591

Serial Number:	77213573	DESIGN FOR POWER
Serial Number:	77213536	SMARTSOURCE
Serial Number:	77395049	WHAT COLOR IS YOUR RTL?
Serial Number:	77469301	POWERCANVAS
Serial Number:	77343496	VECTOR SELECTOR
Serial Number:	77372416	POWERARTIST
Serial Number:	77372263	IT'S COOL TO BE GREEN
Serial Number:	77338082	SEQUENCE DESIGN

CORRESPONDENCE DATA

Fax Number: (214)978-3099

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Email: scarlett.k.pereida@bakemet.com

Correspondent Name: Baker & McKenzie LLP

Address Line 1: 2001 Ross Avenue, Suite 2300

Address Line 4: Dallas, TEXAS 75201

ATTORNEY DOCKET NUMBER:	68166426-001012
NAME OF SUBMITTER:	William D. McSpadden
Signature:	/William D. McSpadden/
Date:	09/09/2009

Total Attachments: 15

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INTELLECTUAL PROPERTY RELEASE

THIS INTELLECTUAL PROPERTY RELEASE (this "Release") is made as of September 4, 2009, by Focus Ventures II, LP, the collateral agent (the "Collateral Agent") under that certain Intellectual Property Security Agreement, dated as of February 11, 2009 (the "IP Security Agreement") by and between Sequence Design, Inc., a California corporation (together with its successors and assigns, the "Company") and the Collateral Agent, in its capacity as representative and collateral agent for and on behalf of the Lenders. Capitalized terms used herein and not otherwise defined shall have the meanings assigned to them in the IP Security Agreement.

WITNESSETH:

WHEREAS, the Collateral Agent and the Company are parties to the IP Security Agreement, pursuant to which the Company has granted a security interest to the Collateral Agent, for itself and on behalf of, and for the ratable benefit of, each of the Lenders, in certain intellectual property (the "Intellectual Property Collateral"), as security for certain obligations owing by the Company to the Collateral Agent and the Lenders party thereto under a Note Purchase and Security Agreement, dated as of February 11, 2009, as amended, modified or supplemented from time to time, including without limitation the specific Intellectual Property Collateral set forth on Exhibits A through D hereto;

WHEREAS, the IP Security Agreement was recorded by the United States Patent and Trademark Office on March 18, 2009, at Reel 022416, Frame 0026, with respect to U.S. Patents (or Patent Applications) of the Company set forth on Exhibit A hereto and at Reel 003955, Frame 0247, with respect to Registered Trademarks and U.S. Pending Trademark Applications of the Company set forth on Exhibits B through C hereto;

WHEREAS, the Company has requested that the Collateral Agent release its security interests in the Intellectual Property Collateral.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged:

1. The Collateral Agent hereby terminates, cancels and releases its security interest in all of the Company's right, title and interest in and to all of the following, all rights in and to which shall immediately revert to the Company, and its successors, legal representatives and assigns, including, without limitation, the specific Intellectual Property Collateral set forth on Exhibits A through D hereto:

- (a) all intellectual property rights of any nature or character including, without limitation, and whether domestic or foreign: (i) all patents and patent applications, all licenses in respect to any rights identified in this clause (a)(i) and all income and royalties with respect to any licenses, all rights to sue for past, present or future infringement of any of the rights identified in this clause (a)(i), all rights arising from any of the rights identified in this clause (a)(i) and pertaining thereto and all reissues, divisions,

continuations, renewals, extensions and continuations-in-part of any of the foregoing; (ii) all copyrights and applications for copyright, together with the underlying works of authorship (including titles), whether or not the underlying works of authorship have been published and whether said copyrights are statutory or arise under the common law, and whether registered or unregistered, and all other rights and works of authorship, all rights, claims and demands in any way relating to any such copyrights or works, including royalties and rights to sue for past, present or future infringement, and all rights of renewal and extension of copyright, and all licenses in respect of any of the rights identified in this clause (a)(ii) and all income and royalties with respect to any such licenses; (iii) all state (including common law), federal and foreign trademarks, service marks and trade names, and applications for registration of such trademarks, service marks and trade names, all licenses relating to any of the rights identified in this clause (a)(iii) and all income and royalties with respect to any licenses, whether registered or unregistered and wherever registered, all rights to sue for past, present or future infringement or unconsented use thereof, all rights arising therefrom and pertaining thereto and all reissues, extensions and renewals thereof; (iv) all regulatory approvals, consents, permits, licenses and applications in respect of any of the foregoing and all supporting documentation, books and records relating to any of the foregoing; and (v) all trade secrets, trade dress, trade styles, logos, other sources of business identifiers, mask-works, mask-work registrations, mask-work applications, software, confidential information, the benefit of confidentiality agreements or non-disclosure agreements, customer lists, license rights (whether or not in respect of any of the rights identified in this clause (a)), advertising materials, operating manuals, methods, processes, know-how, algorithms, formulae, databases, quality control procedures, product, service and technical specifications, operating, production and quality control manuals, sales literature, drawings, specifications, blueprints, descriptions, inventions, name plates and catalogs (the foregoing rights and interests, collectively, the "Intellectual Property Rights") and including, without limitation, those Intellectual Property Rights listed, from time to time, on the Exhibits to this Agreement;

(b) the entire goodwill of or associated with the businesses now or hereafter conducted by the Company connected with and symbolized by any of the aforementioned properties and assets;

(c) all general intangibles and all intangible intellectual or other similar property of the Company of any kind or nature and not otherwise described above;

(d) all products and proceeds at any time of any and all of the foregoing including products of products and proceeds of proceeds; and

(e) with respect to subsections (a) through (d) above, any rights to any new Intellectual Property Rights, or any rights or benefits with respect to any reissue, division, continuation, renewal, extension or continuation-in-part of any Intellectual Property Rights, or any improvement of any Intellectual Property Rights, which Intellectual Property Rights, if existing as of the effective date of the IP Security Agreement, would have been included in subsections (a) through (d) above.

2. Collateral Agent hereby authorizes and requests the Director of the Patent & Trademark Office of the United States of America and the appropriate officers of all other jurisdictions in which any of the Intellectual Property Collateral is in force, or for which application or registration has been made, to record this Release to demonstrate the release by the Collateral Agent of the security interest in the Company's Intellectual Property Collateral, under the relevant laws of the United States or any other jurisdictions.

3. The Collateral Agent will execute and deliver, or cause to be executed and delivered, any other or additional releases, documents, certificates, powers or other writings, and take all additional actions, as may be necessary to record this Release of the Intellectual Property Collateral, to effectuate and validate this Release.

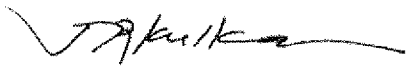
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IN WITNESS WHEREOF, Collateral Agent has caused this Release to be executed as of the day and year first above written.

FOCUS VENTURES II, LP,
as Collateral Agent

By: _____
Name: _____
Title: _____

SEQUENCE DESIGN, INC.,
a California corporation

By:  _____
Name: Vic R. Kulkarni
Title: President

Signature Page to Intellectual Property Release

TRADEMARK
REEL: 004058 FRAME: 0768

EXHIBIT A
to
INTELLECTUAL PROPERTY RELEASE

U.S. Patents (or Patent Applications) of the Company

See attached.

EXHIBIT A

U.S. Patents (or Patent Applications) of Company

Country:	Patent No.:	Issue Date:	Title:	Application No.:	Filing Date:	Status:	Patent No.:	Issue Date:
USA	6,598,209	7/22/2003	RTL Power Analysis Using Gate-Level Cell Power Models	09/798,016	2/28/2001	GRANTED	6,598,209	7/22/2003
USA	6,901,565	5/31/2005	RTL Power Analysis Using Gate-Level Cell Power Models	10/447,076	5/27/2003	GRANTED	6,901,565	5/31/2005
USA	6,574,787	6/3/2003	Method and Apparatus for Logic Synthesis (Word-Oriented Neilist)	09/375,836	8/16/1999	GRANTED	6,574,787	6/3/2003
USA	6,493,648	12/10/2002	Method and Apparatus for Logic Synthesis (Inferring Complex Components)	09/375,254	8/16/1999	GRANTED	6,493,648	12/10/2002
USA	6,698,006	2/24/2004	Method for Balanced-Delay Clock Tree Insertion	10/023,329	12/14/2001	GRANTED	6,698,006	2/24/2004
USA	6,701,505	3/2/2004	Circuit Optimization for Minimum Path Timing Violations	10/008,458	11/30/2001	GRANTED	6,701,505	3/2/2004
USA	7,222,318	5/22/2007	Circuit Optimization For Minimum Path Timing Violations	10/627,933	7/25/2003	GRANTED	7,222,318	5/22/2007
USA	6,519,755	2/11/2003	Method and Apparatus Logic Synthesis With Elaboration	09/375,843	8/16/1999	GRANTED	6,519,755	2/11/2003
USA	6,701,507	3/2/2004	Method for Determining a Zero-Skew Buffer Insertion Point	10/022,751	12/14/2001	GRANTED	6,701,507	3/2/2004
USA	6,701,506	3/2/2004	Method for Match Delay Buffer Insertion	10/022,743	12/14/2001	GRANTED	6,701,506	3/2/2004
USA	6,754,877	6/22/2004	Method for Optimal Driver Selection	10/022,747	12/14/2001	GRANTED	6,754,877	6/22/2004
USA	7,003,741	2/21/2006	Method For Optimal Driver Selection	10/838,811	5/3/2004	GRANTED	7,003,741	2/21/2006

Country:	Patent No.:	Issue Date:	Title:	Application No.:	Filing Date:	Status:	Patent No.:	Issue Date:
USA	6,807,660	10/19/2004	Vectorless Instantaneous Current Estimation	10/262,914	10/1/2002	GRANTED	6,807,660	10/19/2004
USA	7,185,300	2/27/2007	Vectorless Instantaneous Current Estimation	10/926,660	8/25/2004	GRANTED	7,185,300	2/27/2007
USA	7,117,457	10/3/2006	Current Scheduling System And Method For Optimizing Multi-Threshold CMOS Designs	10/739,659	12/17/2003	GRANTED	7,117,457	10/3/2006
TAIW			Design Method And Architecture For Power Gate Switch Placement	94129877	8/31/2005	Filed		
USA			Design Method And Architecture For Power Gate Switch Placement	10/998,204	11/26/2004	Filed		
USA			Design Method That Allows Flexible Evaluation Of Power Gated Circuits	11/150,031	6/10/2005	Filed		
USA	7,323,909	1/29/2008	Automatic Extension Of Clock Gating Technique To Fine-Grained Power Gating	11/193,149	7/29/2005	GRANTED	7,323,909	1/29/2008
USA			Automatic Extension Of Clock Gating Technique To Fine-Grained Power Gating	11/952,937	12/7/2007	Filed		
USA			Automatic Voltage Drop Optimization	11/551,149	10/19/2006	Filed		
USA			Design Method and Architecture for Power Gate Switch Placement and Interconnection Using Tapless Libraries	11/331,913	1/13/2006	Filed		
USA	5,901,063	5/4/1999	System and Method for Extracting Parasitic Impedance from an Integrated Circuit Layout	08/804,524	2/21/1997	GRANTED	5,901,063	5/4/1999
TAIW	136000	11/1/2001	Methods for Determining On-Chip Interconnect Process Parameters	87115892	9/24/1998	GRANTED	136000	11/1/2001
USA	6,057,171	5/2/2000	Methods for Determining On-Chip Interconnect Process Parameters	08/937,393	9/25/1997	GRANTED	6,057,171	5/2/2000
USA	6,312,963	11/6/2001	Methods for Determining On-Chip Interconnect Process Parameters	09/245,812	2/4/1999	GRANTED	6,312,963	11/6/2001

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Country:	Patent No.:	Issue Date:	Title:	Application No.:	Filing Date:	Status:	Patent No.:	Issue Date:
USA	6,291,254	9/18/2001	Methods for Determining On-Chip Interconnect Process Parameters	09/244,616	2/4/1999	GRANTED	6,291,254	9/18/2001
USA	6,403,369	6/11/2002	Methods for Determining On-Chip Sheet Resistivity	09/373,923	8/12/1999	GRANTED	6,403,369	6/11/2002
USA	6,381,730	4/30/2002	Method and System for Extraction of Parasitic Interconnect Impedance Including Inductance	09/350,966	7/9/1999	GRANTED	6,381,730	4/30/2002
USA	6,643,831	11/4/2003	Method and System for Extraction of Parasitic Interconnect Impedance Including Inductance	10/057,165	1/24/2002	GRANTED	6,643,831	11/4/2003
USA	6,311,312	10/30/2001	Method for Modeling A Conductive Semiconductor Substrate	09/405,510	9/23/1999	GRANTED	6,311,312	10/30/2001
USA	6,591,407	7/8/2003	Method and Apparatus for Interconnect-Driven Optimization of Integrated Circuit Design	09/516,489	3/1/2000	GRANTED	6,591,407	7/8/2003
USA	7,222,311	5/22/2007	Method And Apparatus For Interconnect-Driven Optimization Of Integrated Circuit Design	10/387,644	3/12/2003	GRANTED	7,222,311	5/22/2007

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EXHIBIT B
to
INTELLECTUAL PROPERTY RELEASE

Registered Trademarks of the Company

See attached.

EXHIBIT B

Registered Trademarks of Company:

Country	Mark Name	Application No.	Filing Date	Registration No.	Registered Date	Status
USA	COLLUMBUS	75/109,383	May 24, 1996	2,162,591	June 2, 1998	Registered
USA	POWERTHEATER	78/066,862	June 1, 2001	2,744,939	July 29, 2003	Registered
JAPAN	NANOCOOL	2002-097653	November 19, 2002	4665189	April 18, 2004	Registered
USA	ELMO	76/523,490	June 18, 2003	2,947,349	May 10, 2005	Registered
USA	COOLTIME	76/523,255	June 18, 2003	2,881,000	September 7, 2004	Registered
USA	SHOWTIME	76/557,279	November 5, 2003	2,912,433	December 21, 2004	Registered
USA	PHYSICALSTUDIO	76/557,290	November 5, 2003	2,912,434	December 21, 2004	Registered
USA	EXTRACTIONSTAGE	76/564,875	December 12, 2003	3,003,308	October 4, 2005	Registered
USA	COOLPOWER	78/590,871	March 18, 2005	3225732	April 3, 2007	Registered
USA	WATTWATCHER	78/338,869	August 11, 1995	2252594	August 11, 1995	Registered

EXHIBIT C
to
INTELLECTUAL PROPERTY RELEASE

U.S. Pending Trademark Applications of the Company

See attached.

EXHIBIT C

U.S. Pending Trademark Applications of Company

Country	Mark	Registration No.	Registration Date	Status
USA	CoolTheatre	78/590,841	March 18, 2005	FILED
USA	Cool By Design	78/590,851	March 18, 2005	FILED
USA	CoolCheck	78,822,255	February 23, 2006	FILED
USA	NANOCOOL	78/727,932	October 6, 2005	FILED
USA	Design for Power	77/213573	June 22, 2007	FILED
USA	SMARTSOURCE	77/213536	June 22, 2007	FILED
USA	WHAT COLOR IS YOUR RTL?	77395049	12-Feb-08	FILED
USA	POWERCANVAS	77469301	8-May-08	FILED
USA	VECTOR SELECTOR	77343496	4-Dec-07	FILED
USA	POWERARTIST	77372416	15-Jan-08	FILED
USA	IT'S COOL TO BE GREEN	77372263	15-Jan-08	FILED
USA	SEQUENCE DESIGN	77338082	27-Nov-07	FILED
INHOUSE				
INHOUSE				
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EXHIBIT D
to
INTELLECTUAL PROPERTY RELEASE

Copyright/Mask-PCT Authority Registrations of the Company

See attached.

EXHIBIT D

Copyright/Mask-PCT Authority Registrations of Company:

[None.]